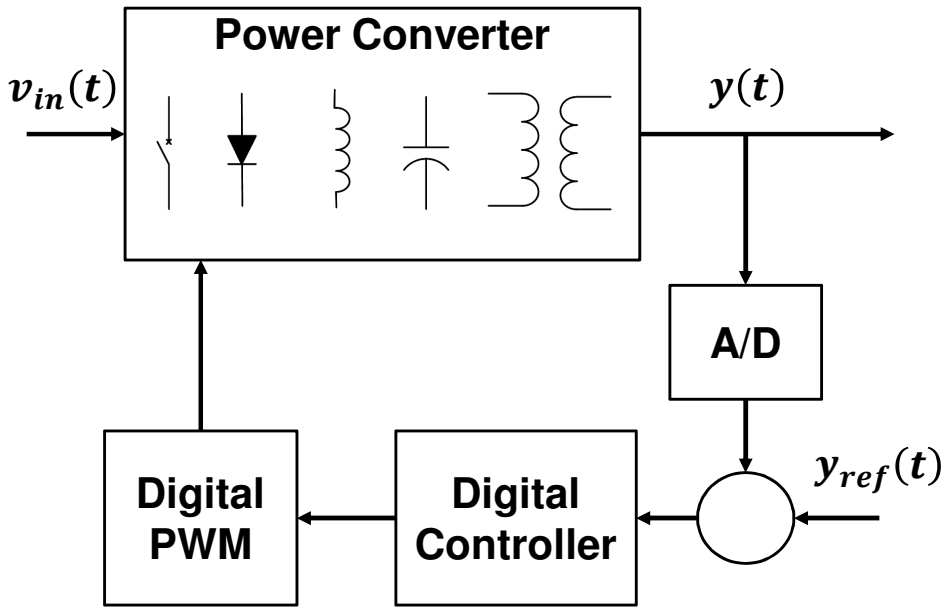
22nd International SPIN Symposium on Model Checking of Software

DSVerifier: A Bounded Model Checking Tool for Digital Systems

Hussama I. Ismail, **Iury V. Bessa**, Lucas C. Cordeiro
Eddie B. de Lima Filho, and João E. Chaves Filho

Digital Systems Applications and Limitations

- Digital filters and controllers are currently replacing many analog components
- Despite several advantages, they present limitations related to **finite-word length** (FWL) effects
- Limit cycle oscillations (LCOs) in power converters:
  - Oscillation in output voltage due to round-off and overflows
  - More **energy losses** and short **silicon lifespan**
  - LCOs are almost unavoidable and difficult to be detected
  - LCOs are typically detected via time-domain simulations



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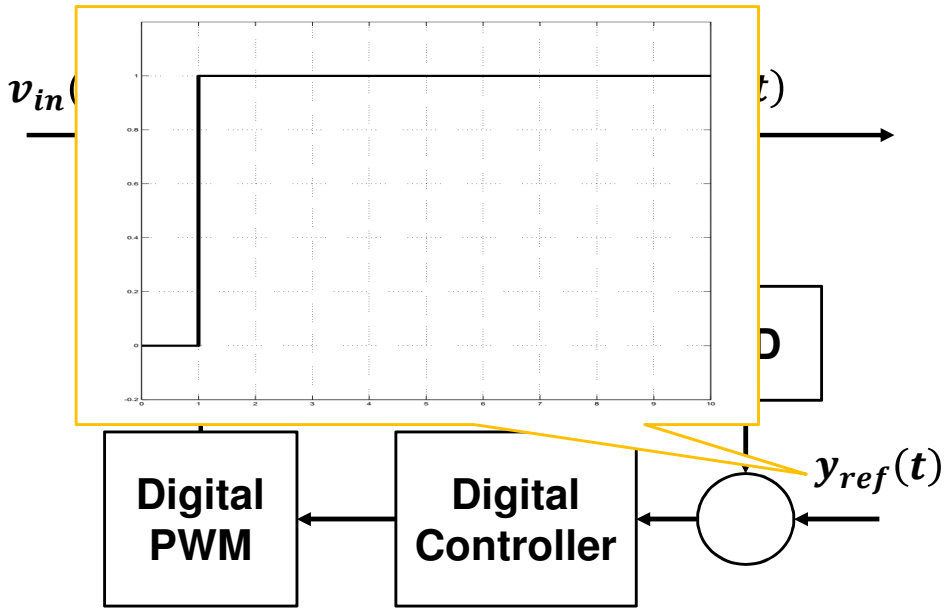

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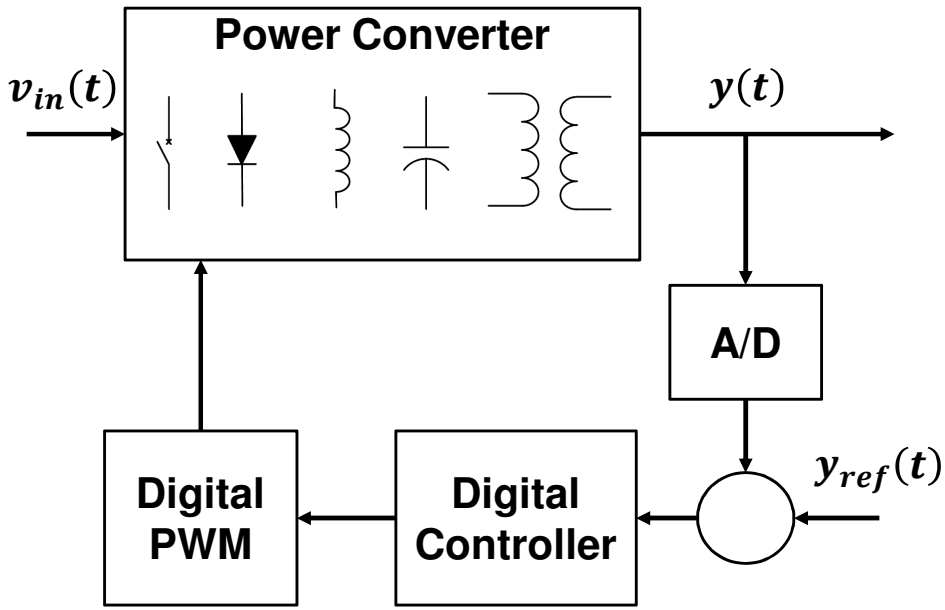

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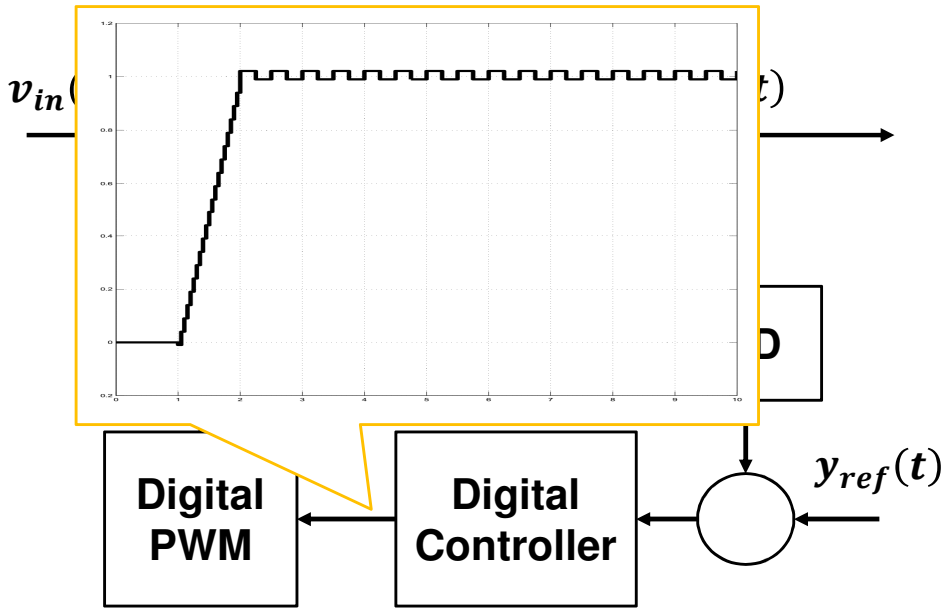

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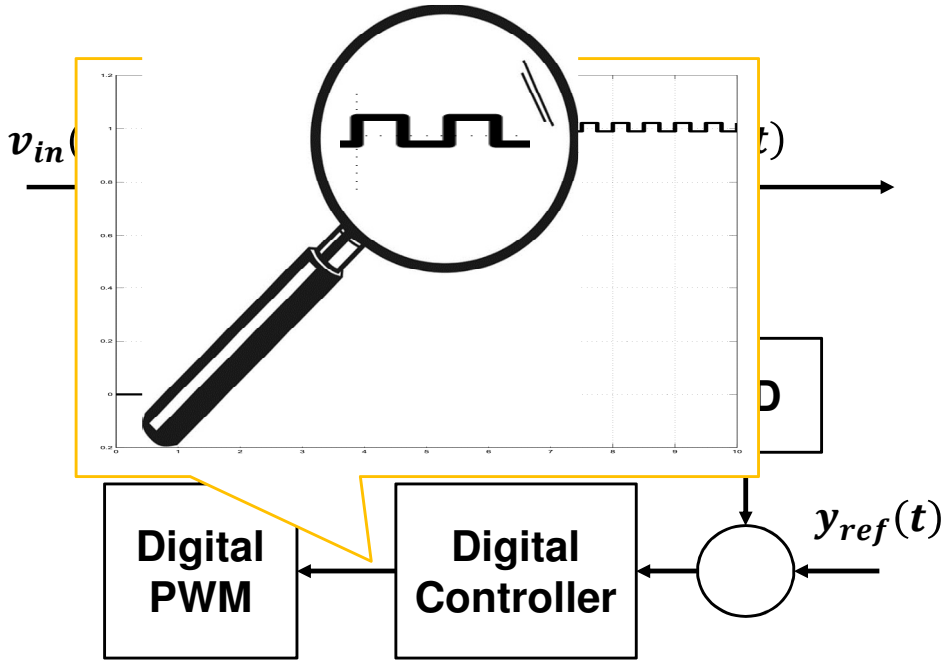

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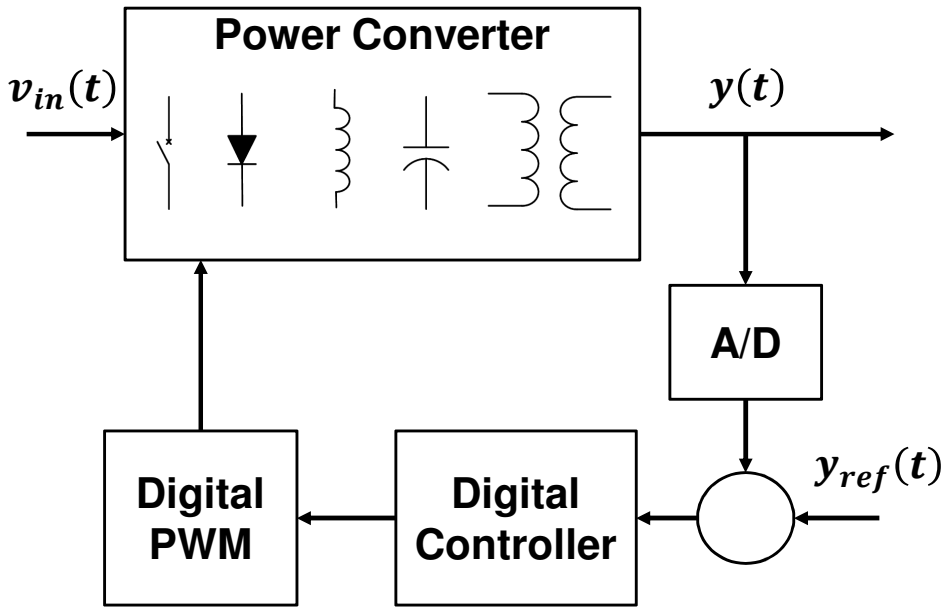

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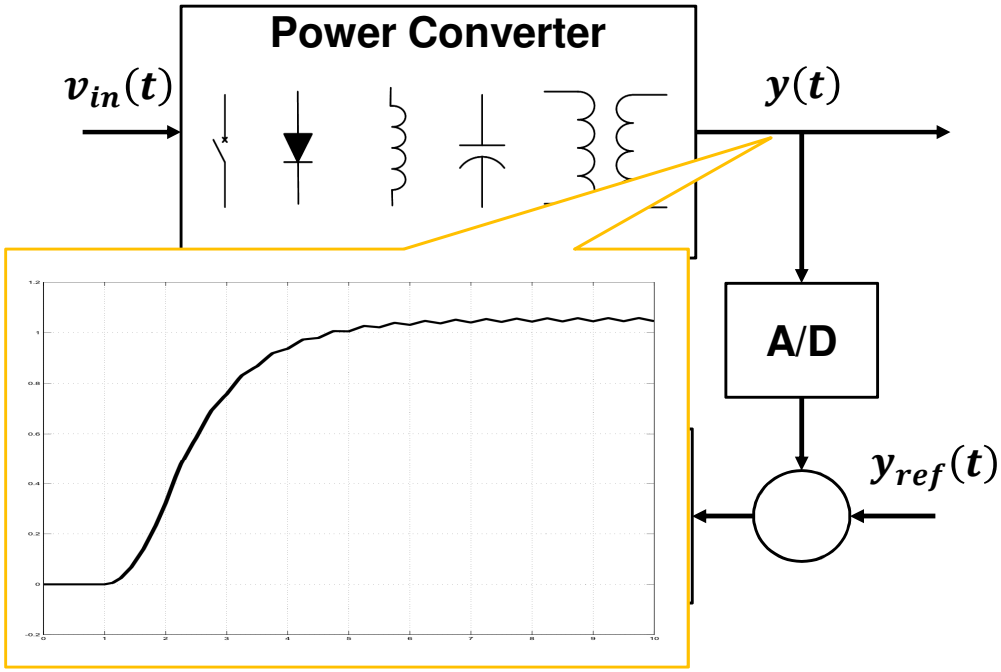

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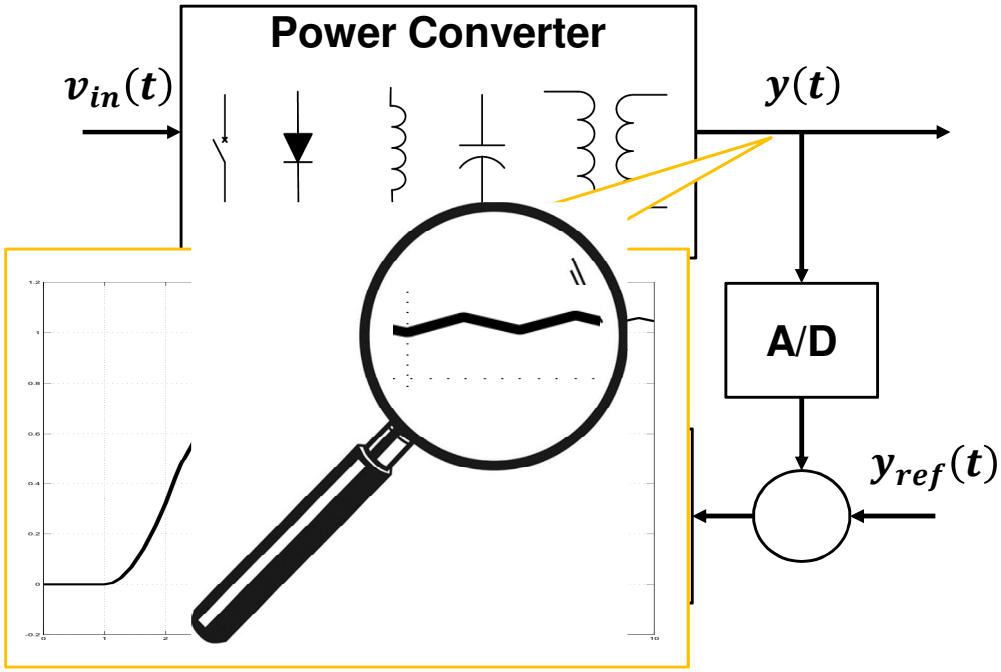

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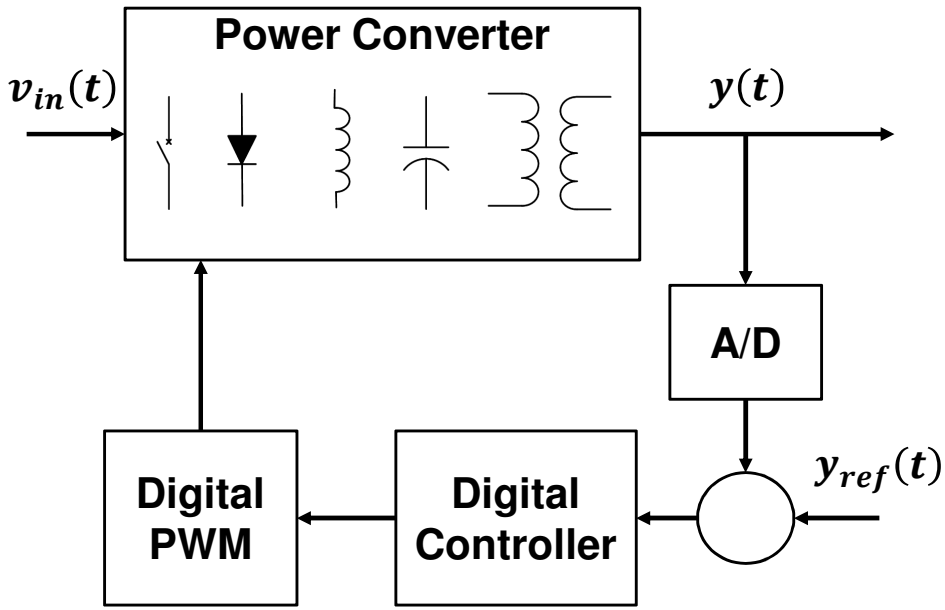
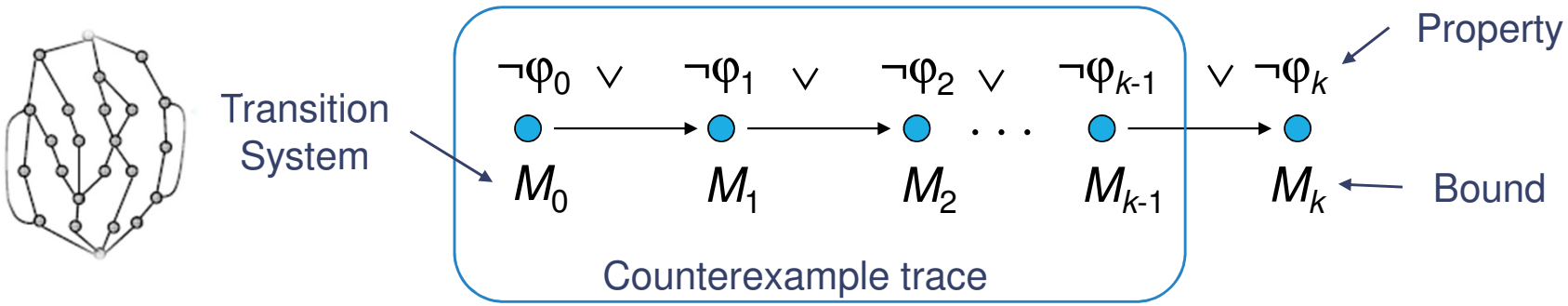


Bounded Model Checking (BMC)

- Basic Idea: given a transition system *M*, check negation of a given property *φ* up to given depth *k*



- Translated into a VC *ψ* such that: ***ψ* is satisfiable iff *φ* has counterexample of max. depth *k***
- BMC has been applied successfully to verify (embedded) software since early 2000's, but it has not been used to verify digital controllers

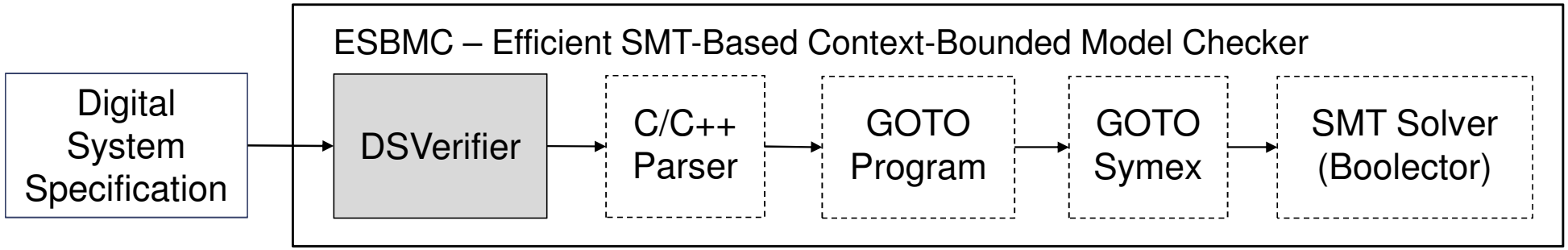
Objectives

BMC of digital systems implementations considering FWL effects

- Investigate FWL effects in fixed-point digital system (controllers and filters) implementations via BMC techniques
- Apply a design-aided verification methodology to digital systems, which is supported by the Digital-Systems Verifier (DSVerifier)
- Verify overflows, limit cycles, time constraints, stability, and mimimum phase in digital systems using standard benchmarks

The Digital-Systems Verifier (DSVerifier)

- DSVerifier is an additional module for the Efficient SMT-based Context-Bounded Model Checker (ESBMC) to add support for digital systems verification



The complete tool includes four components from ESBMC
C Parser, GOTO Program, GOTO Symex, and SMT Solver

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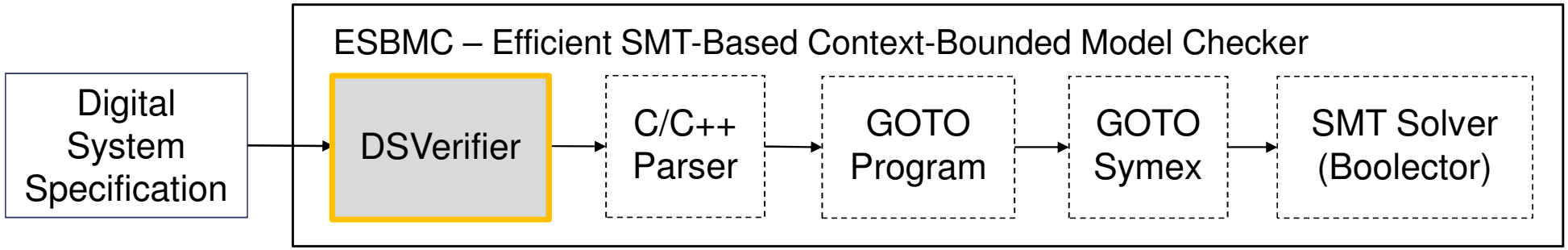

DSVerifier module is included before the ANSI-C parser, which provides functions related to quantization, digital-system realizations, and property verification

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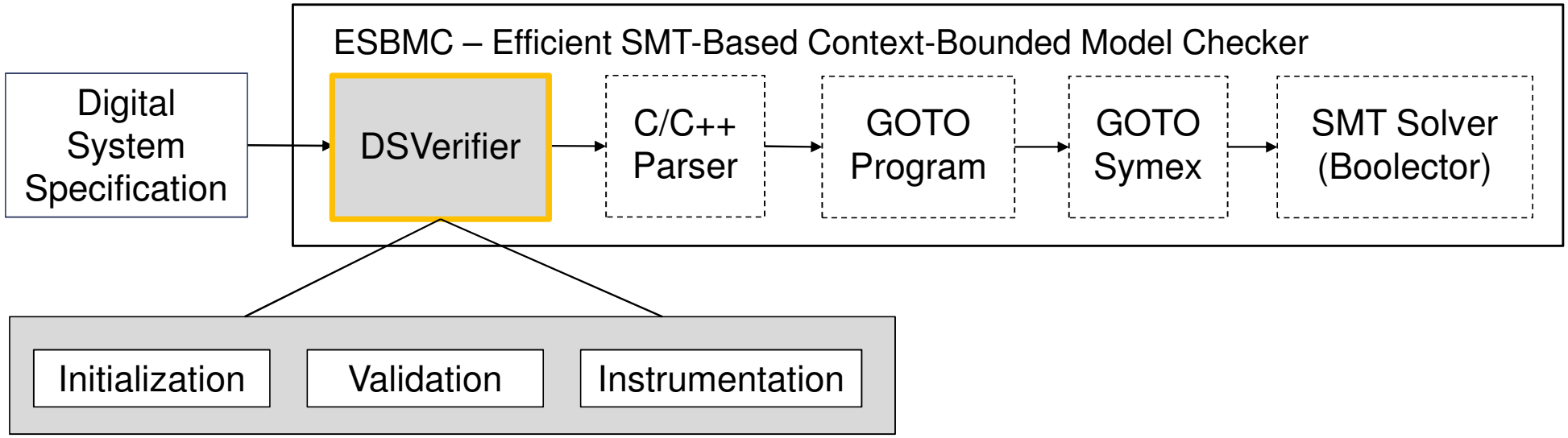

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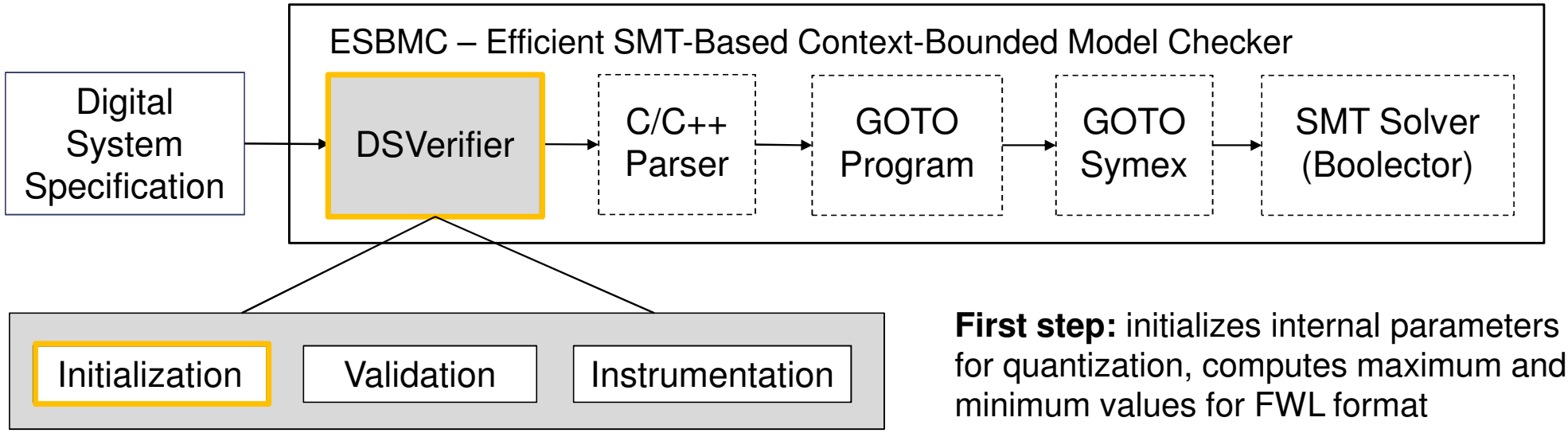

First step: initializes internal parameters for quantization, computes maximum and minimum values for FWL format

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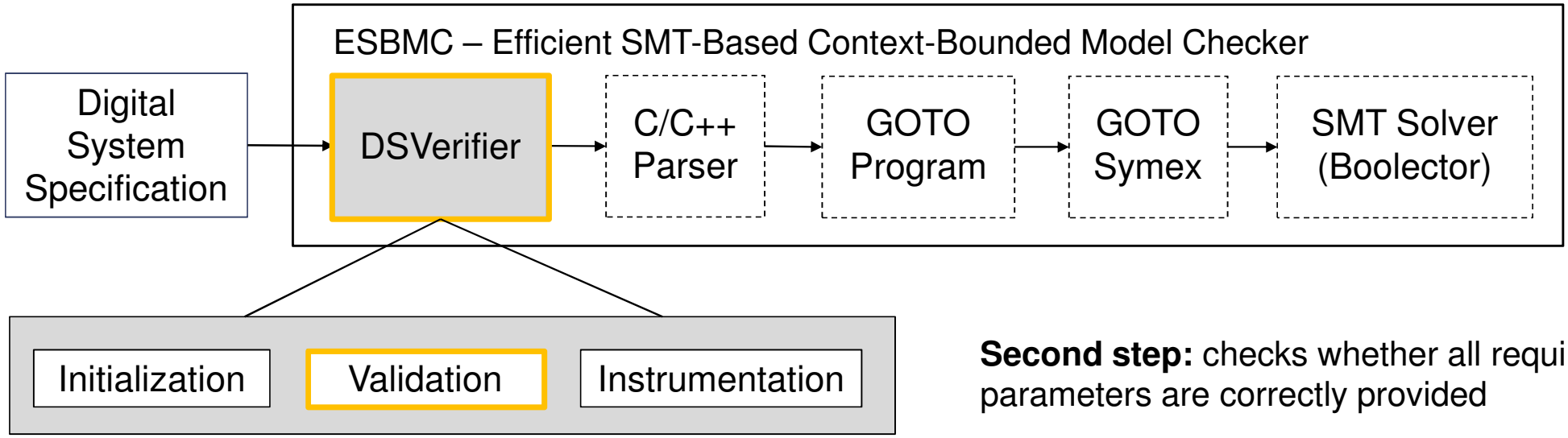

Second step: checks whether all required parameters are correctly provided

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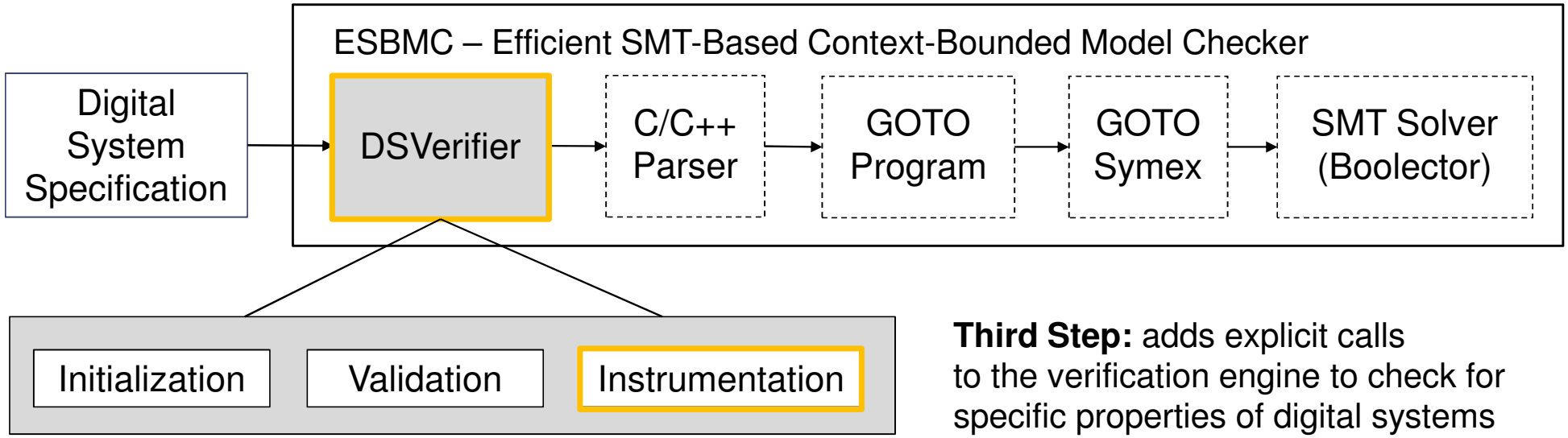

Third Step: adds explicit calls to the verification engine to check for specific properties of digital systems

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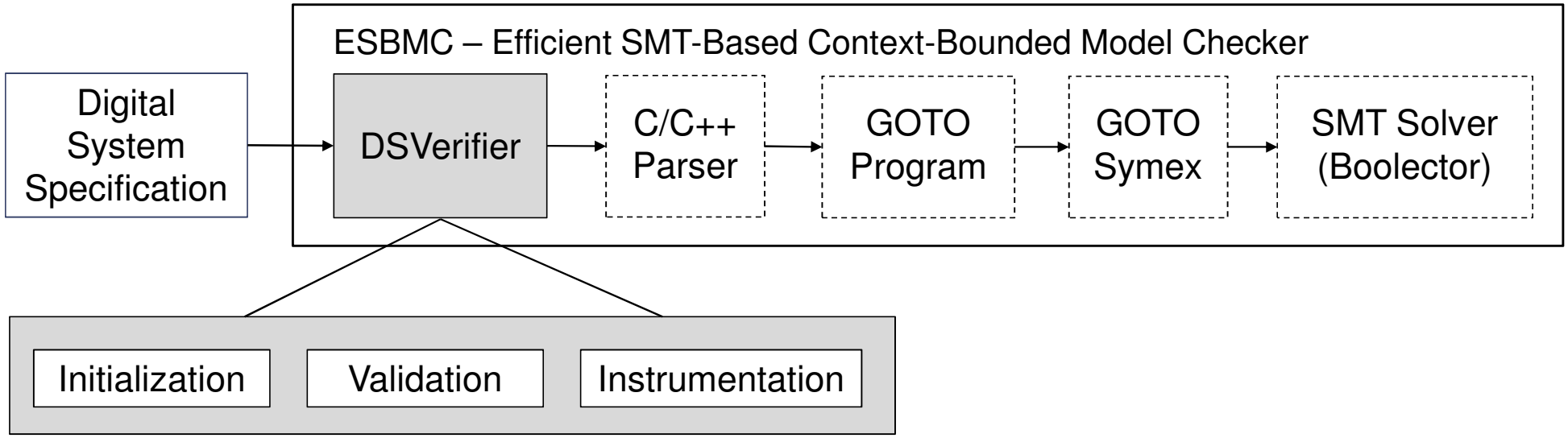

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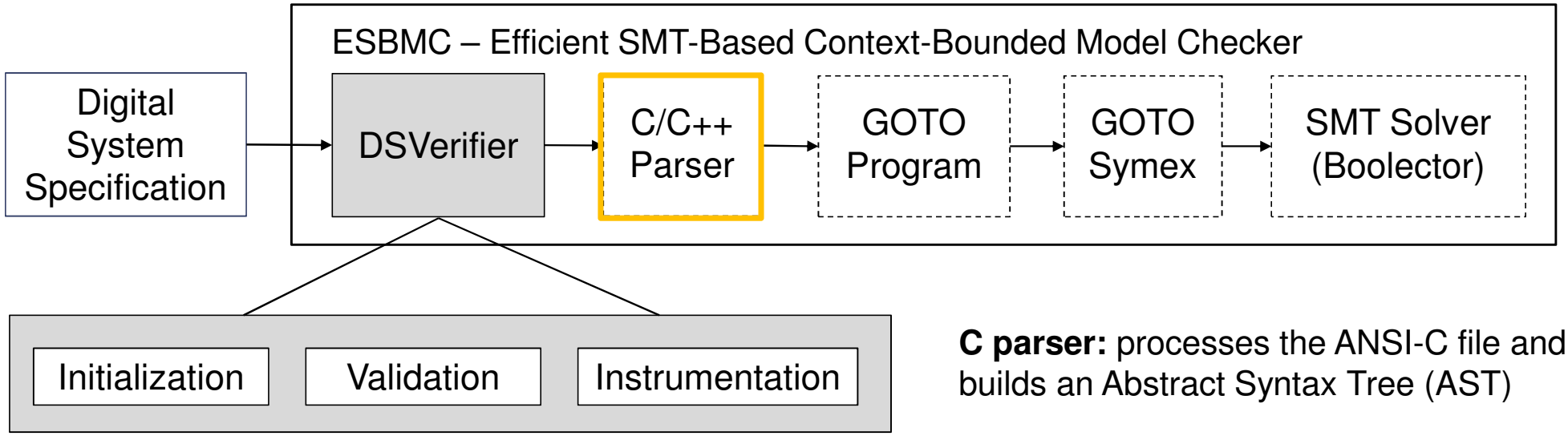

C parser: processes the ANSI-C file and builds an Abstract Syntax Tree (AST)

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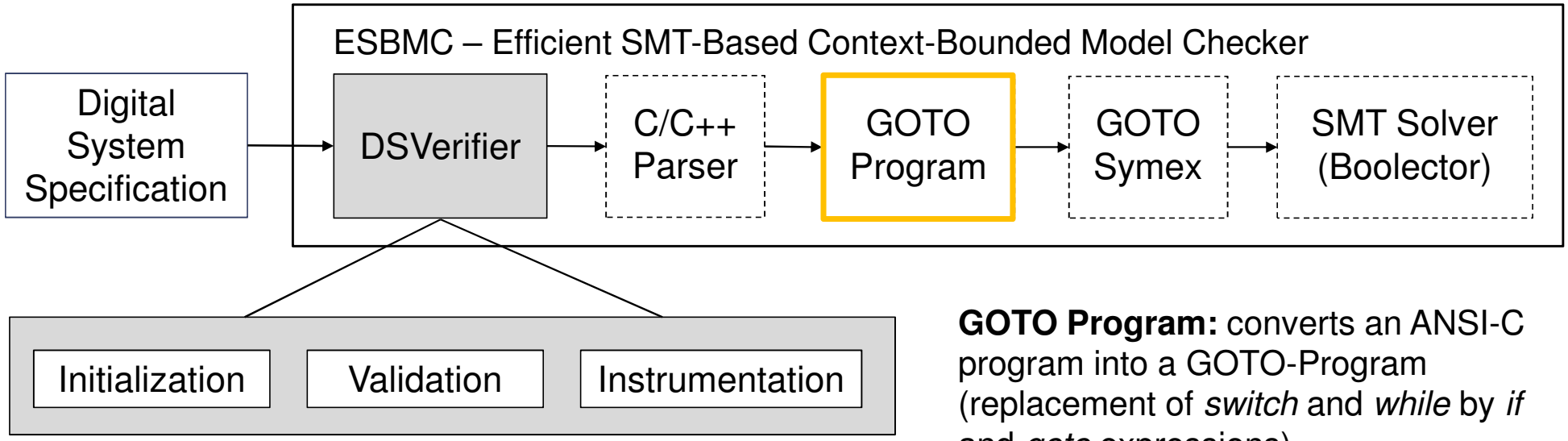

GOTO Program: converts an ANSI-C program into a GOTO-Program (replacement of *switch* and *while* by *if* and *goto* expressions)

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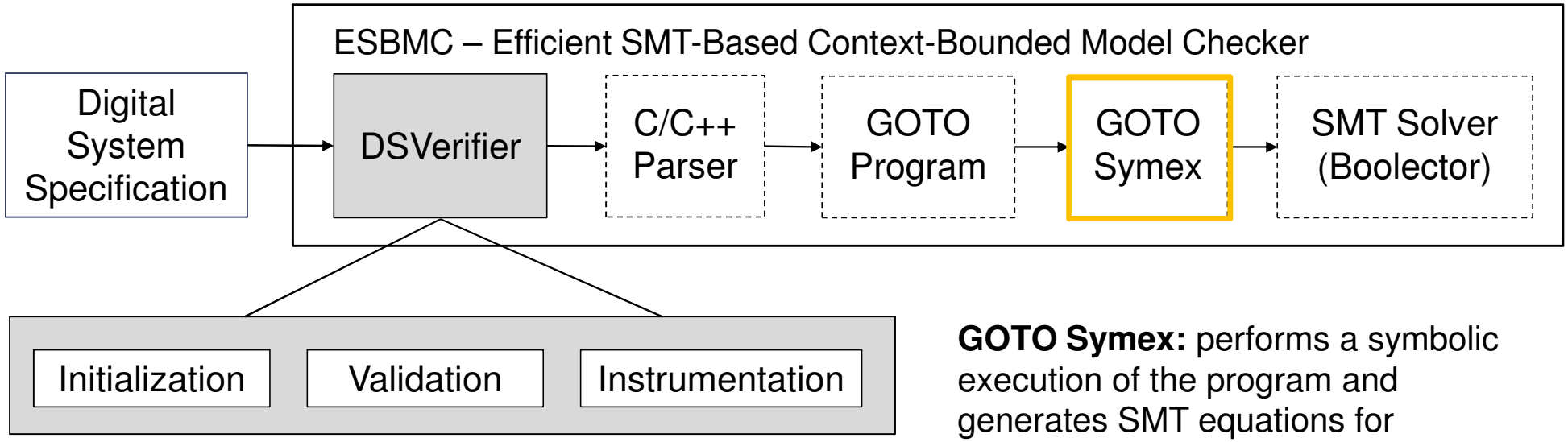

GOTO Symex: performs a symbolic execution of the program and generates SMT equations for constraints (*C*) and properties (*P*)

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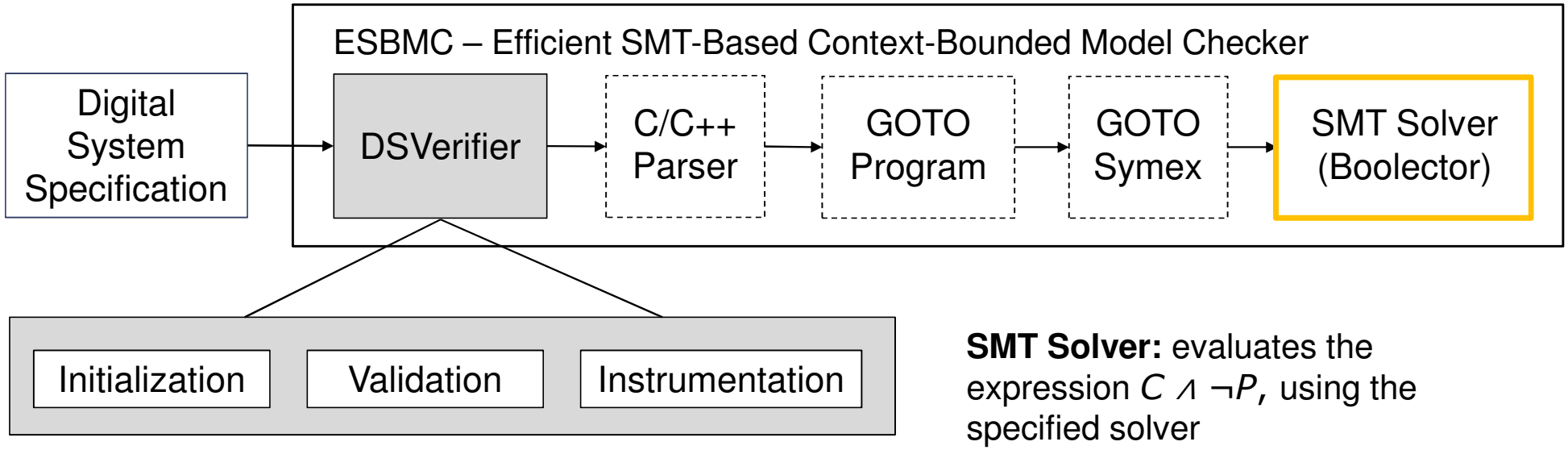

SMT Solver: evaluates the expression $C \wedge \neg P$, using the specified solver

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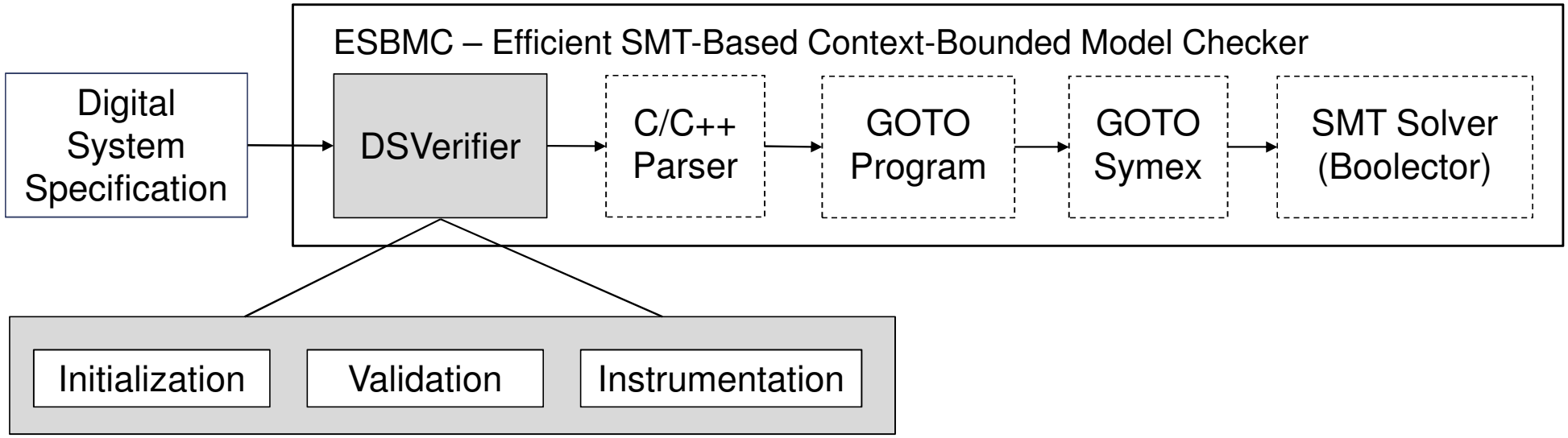
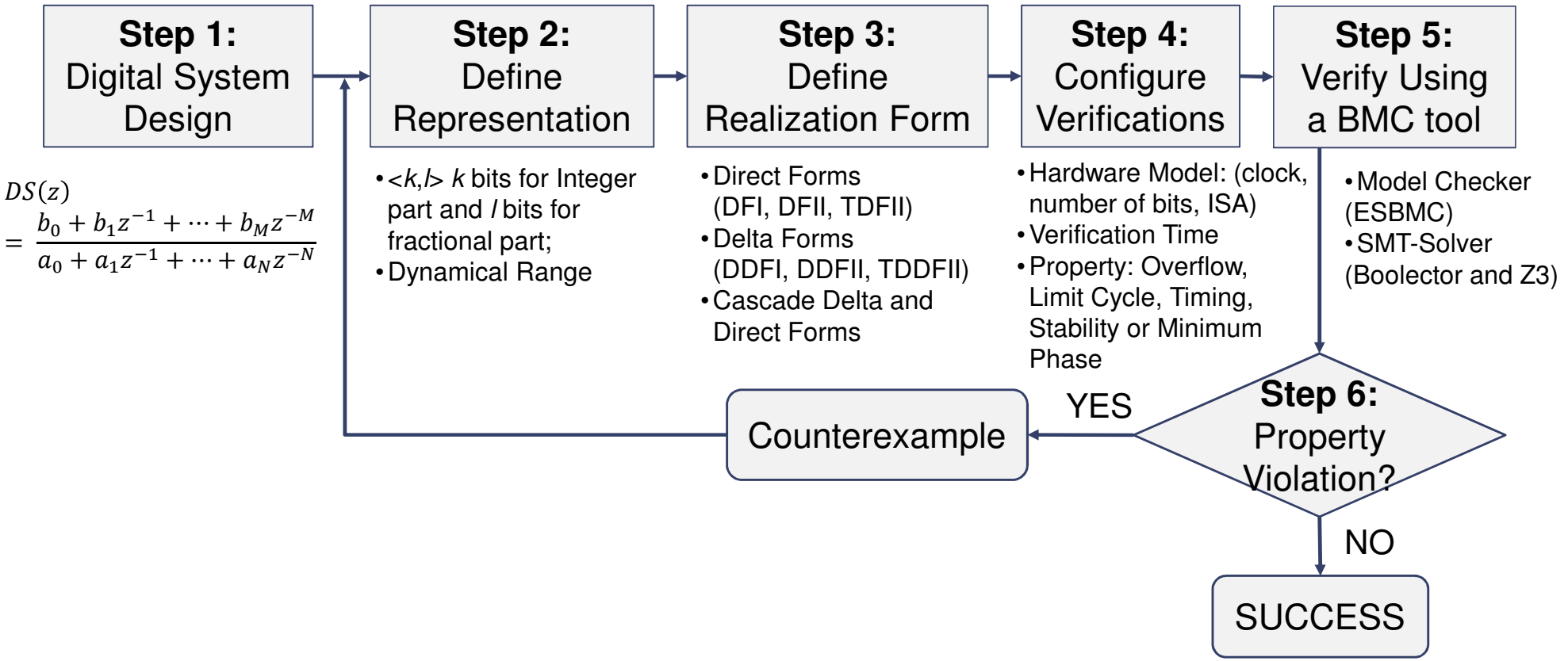


DSVerifier Features

- DSVerifier supports five verification properties, considering three direct- and delta-form implementations, in addition to the cascade form

1. **Overflow:** if a sum or product exceeds the number representation
2. **Limit Cycle:** checks for zero-input limit cycles, for any initial condition
3. **Stability:** considers FWL effects on pole locations
4. **Minimum phase:** considers FWL effects on zero locations
5. **Time constraints:** checks whether a specific realization meets time constraints

DSVerifier-Aided Verification Methodology



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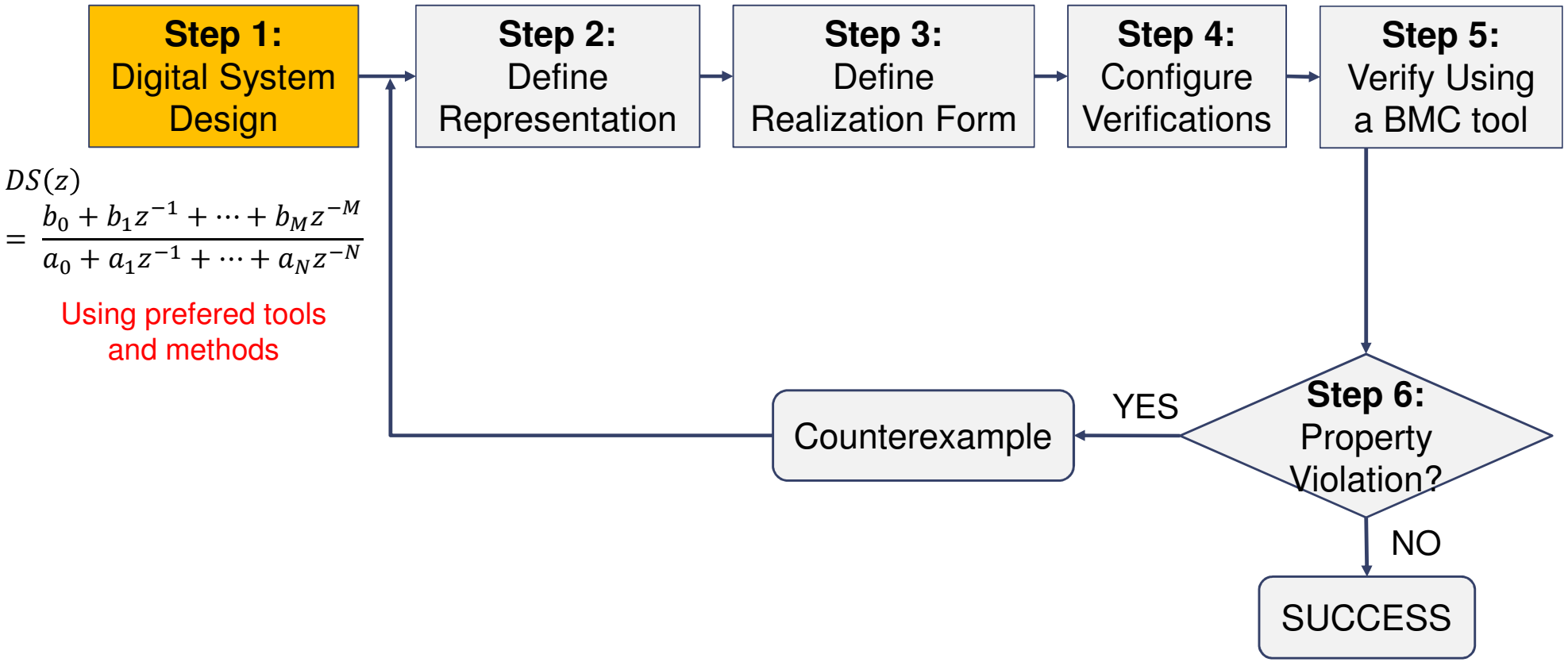

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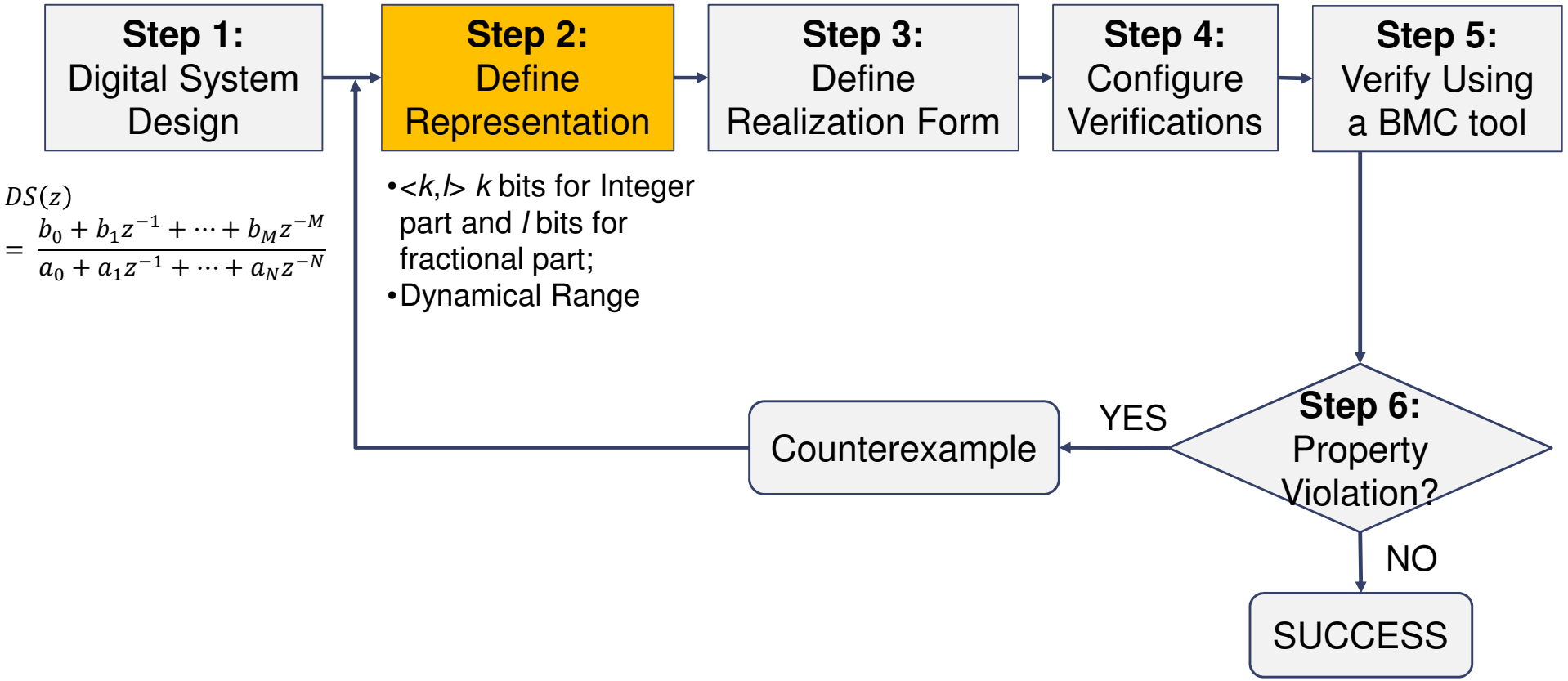

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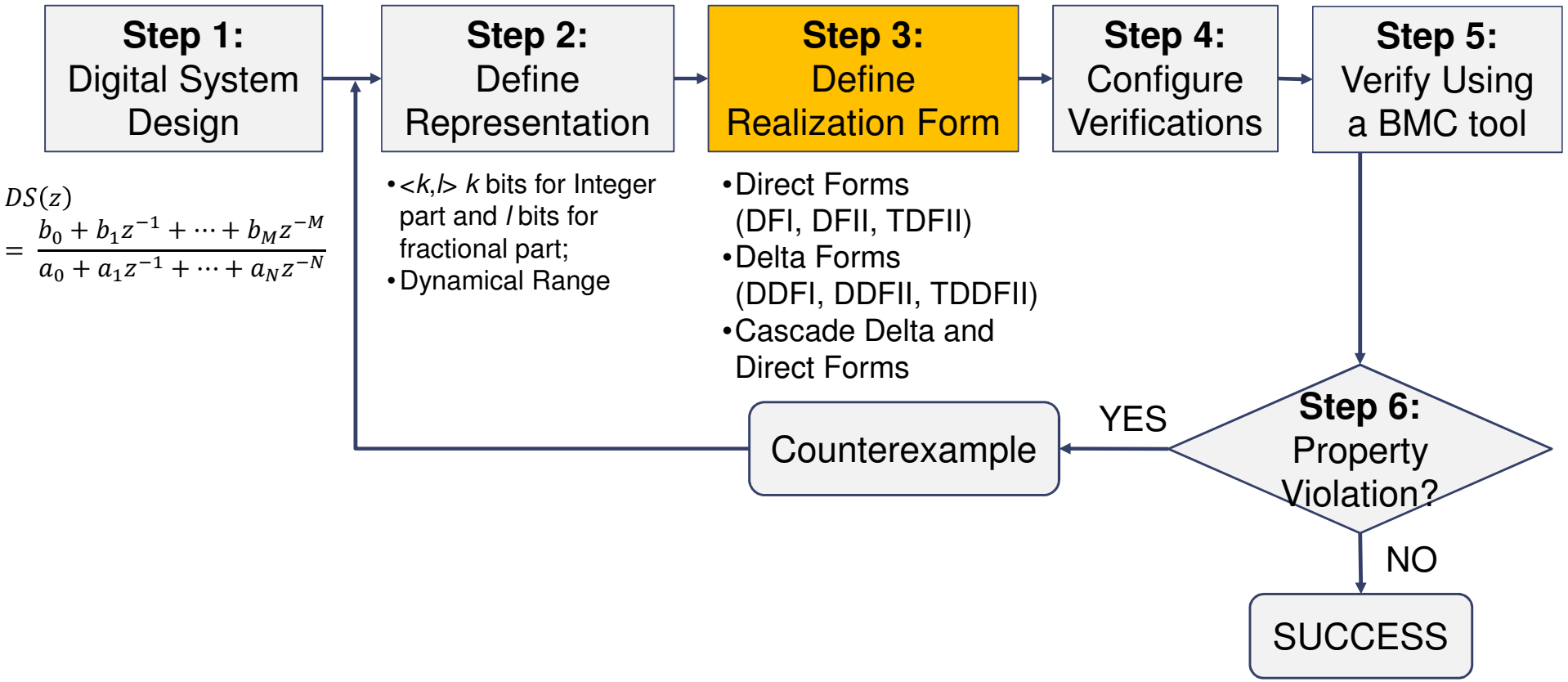

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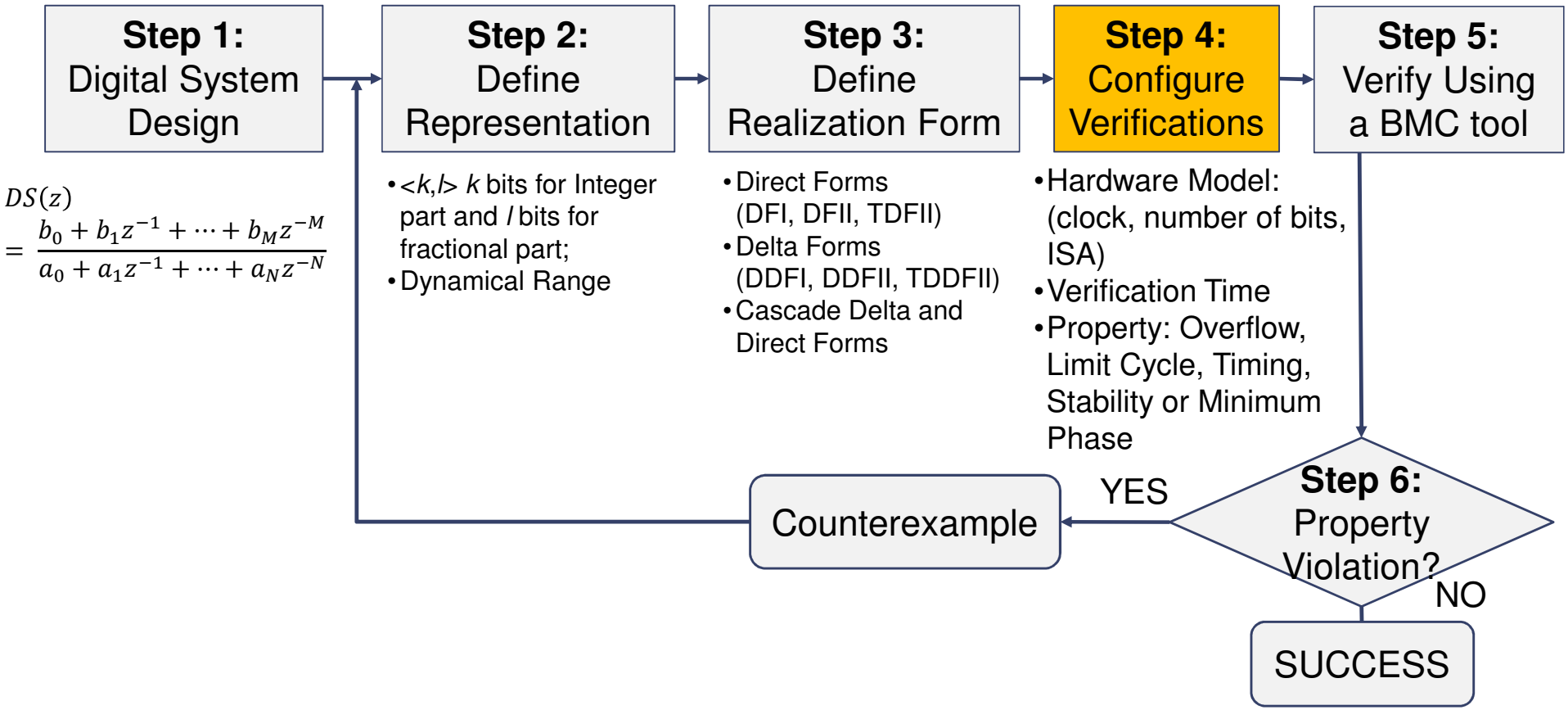

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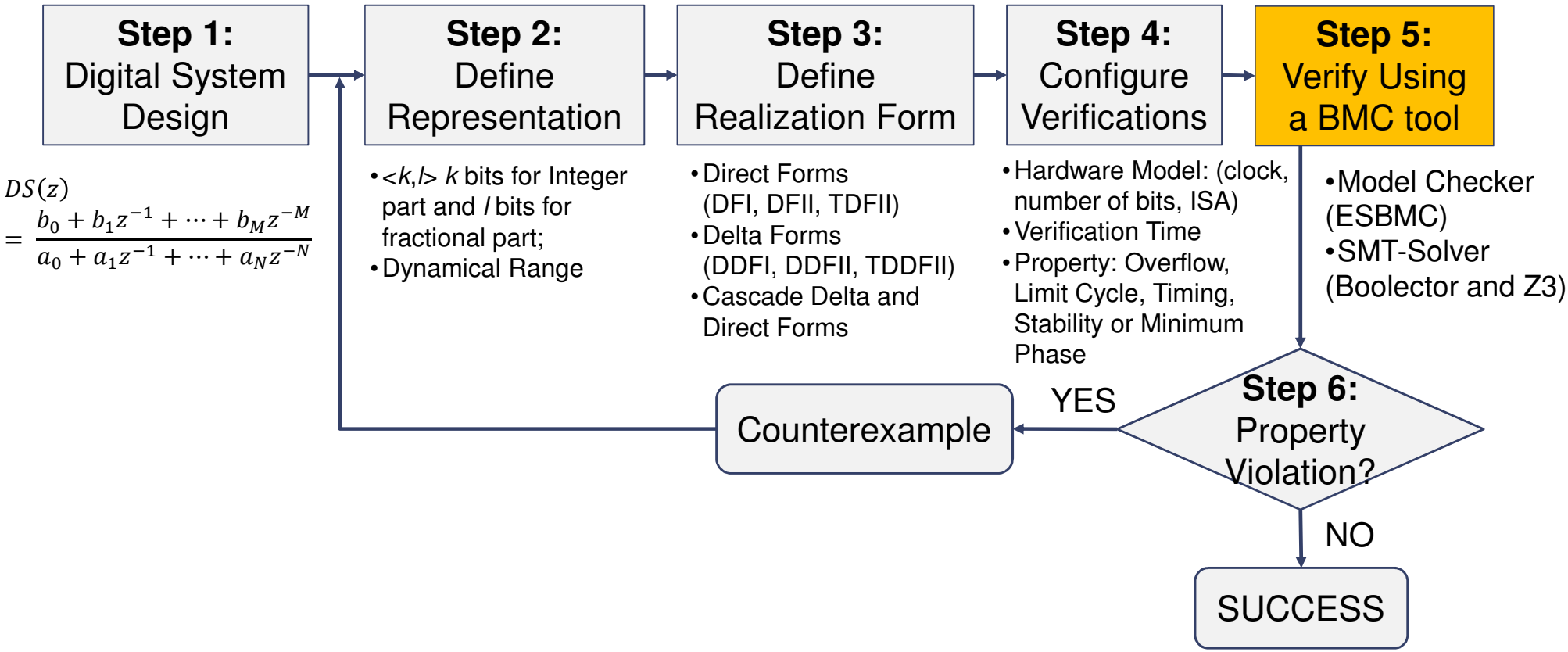

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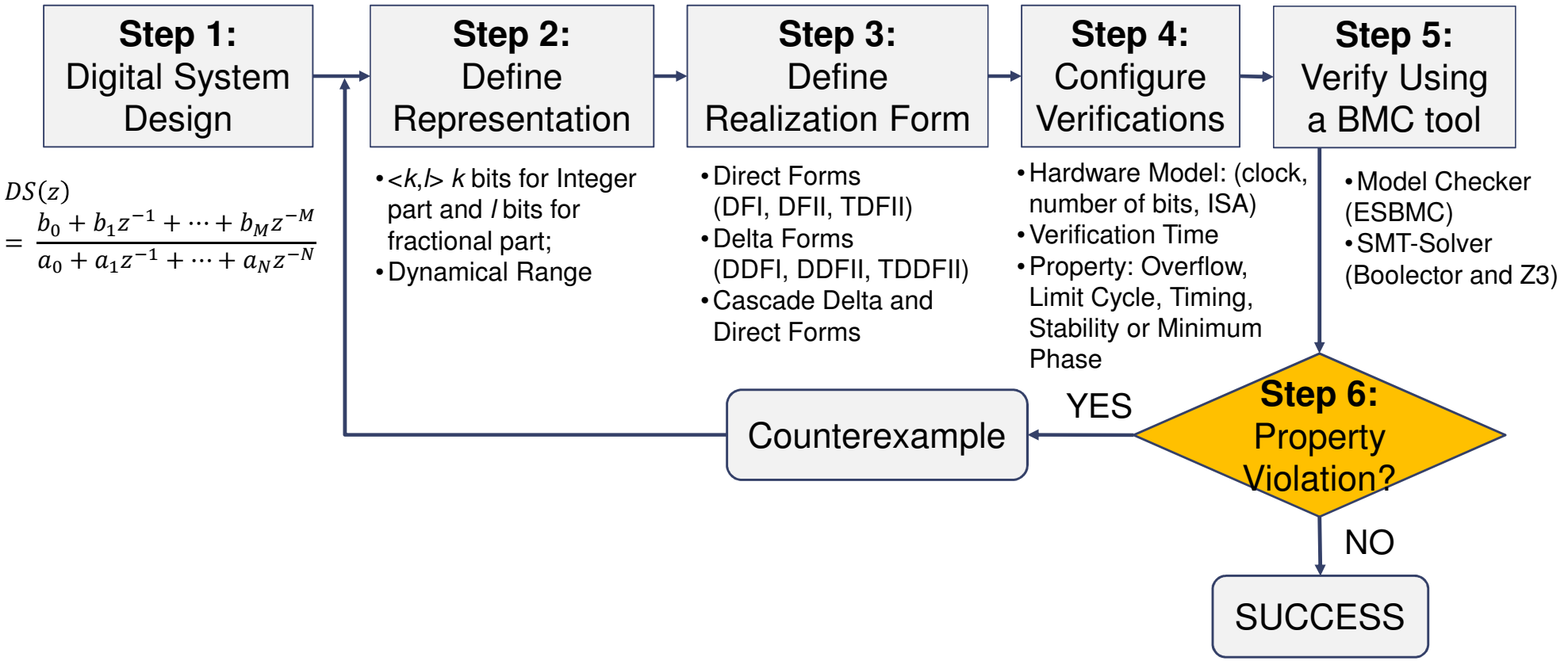

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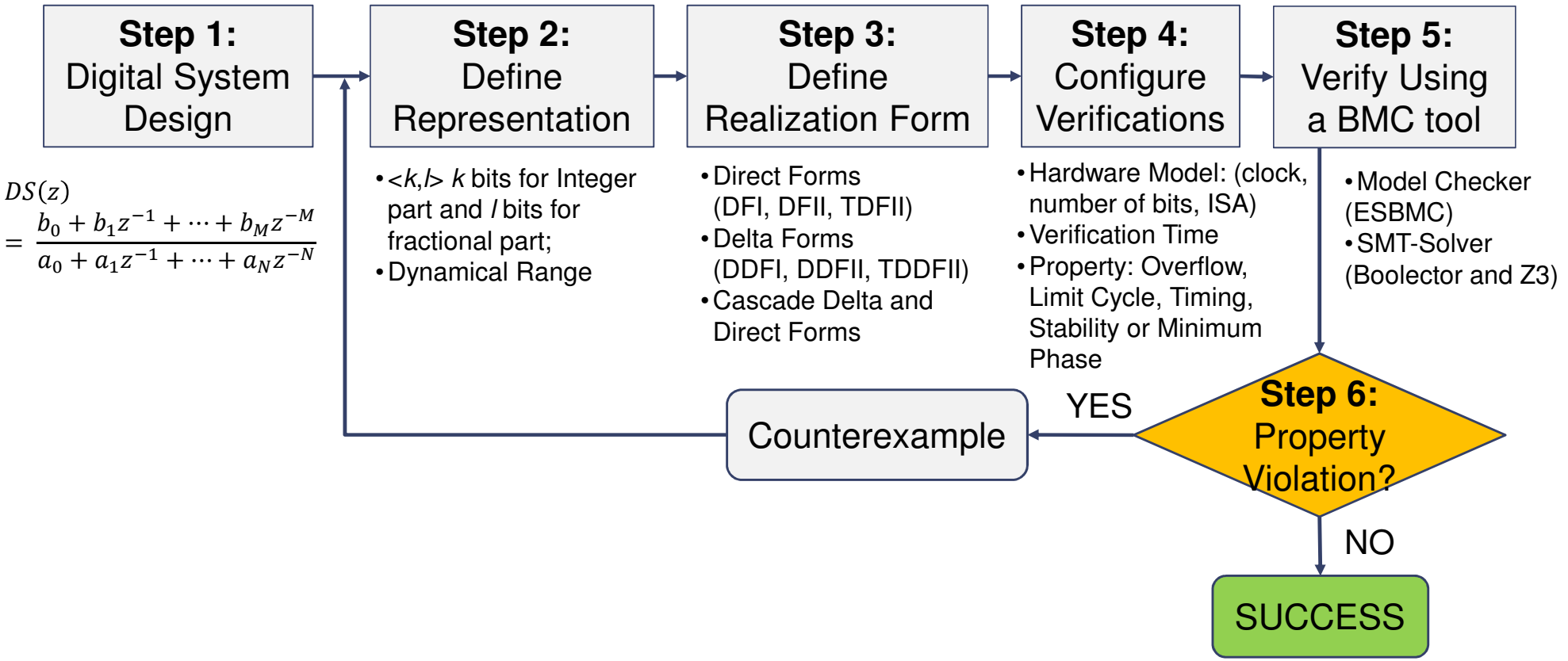

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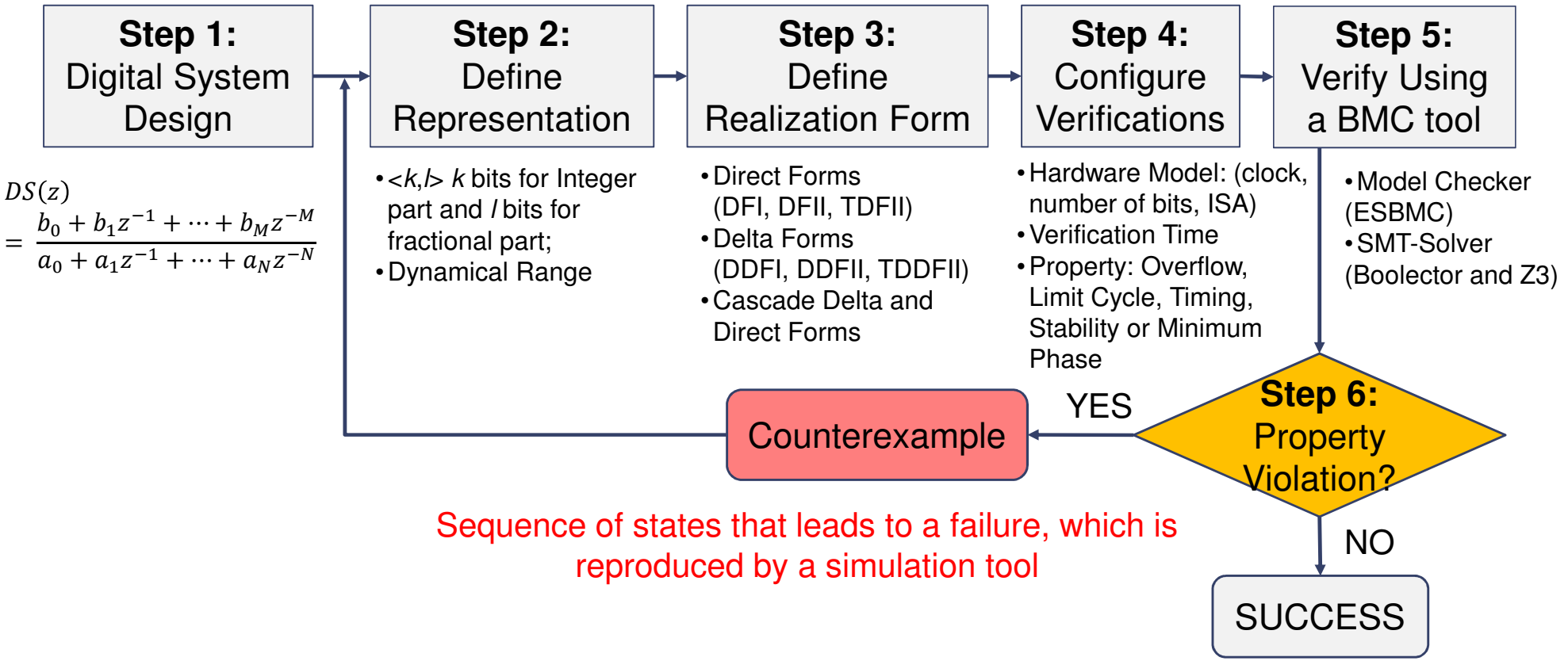

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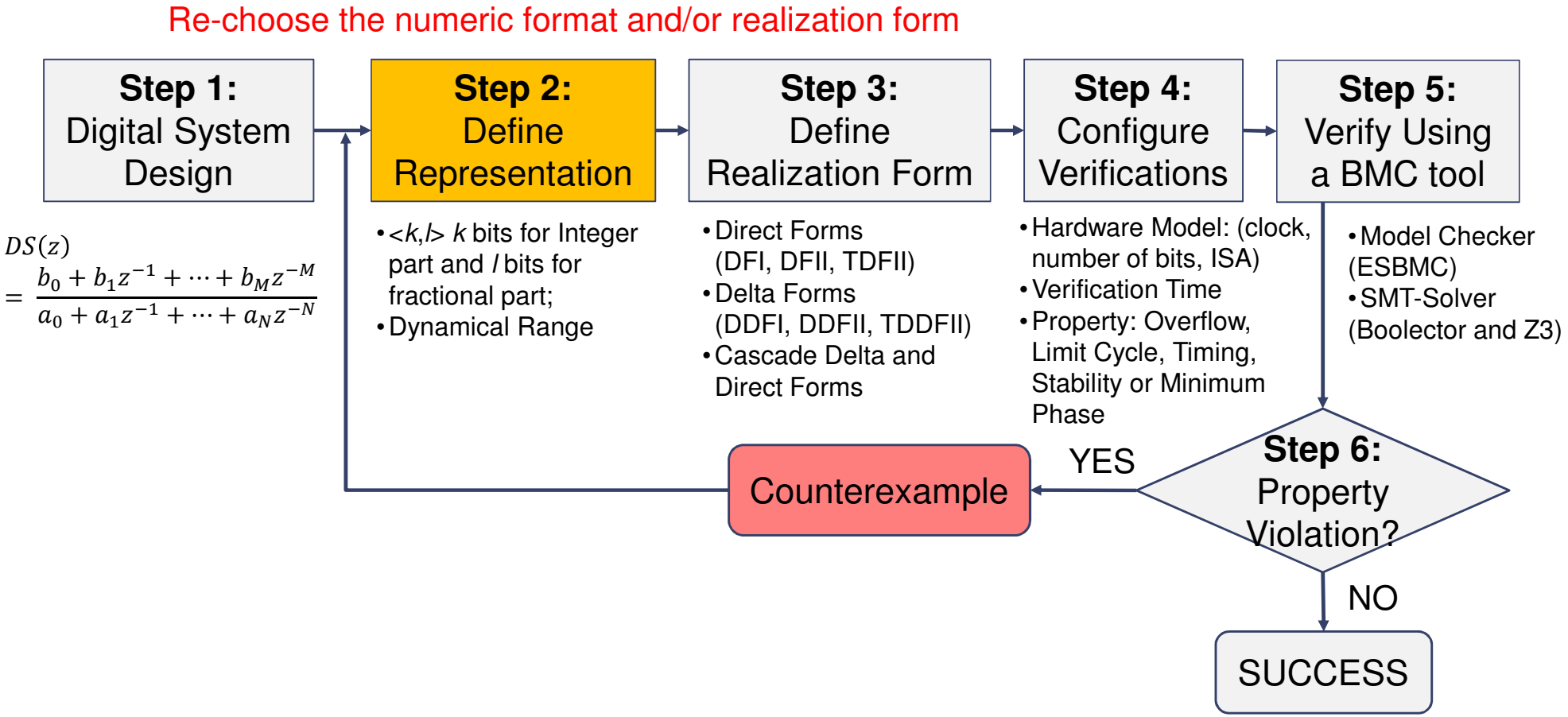

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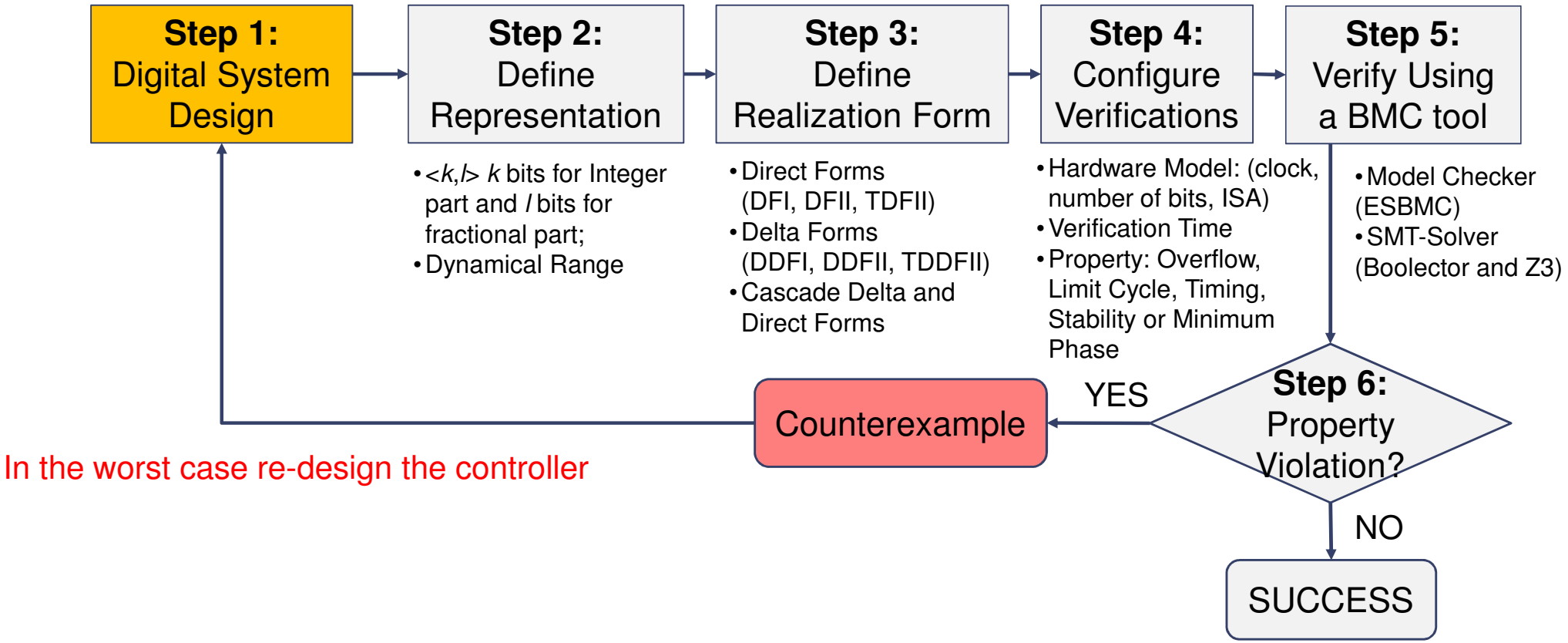

DSVerifier-Aided Verification Example

- $C(z) = \frac{0.2(z^2-2z+1)}{z^2-0.25}$

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- $< 3,12 >$:3 bits for integer part and 12 bits for fractional part
- Dynamical Range: [-1,1]

Numeric format choosen based on impulse response sum and hardware limitations

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- DFII

Random first trial

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- Verify overflow
- Verification time:3600
- MSP430 16-bit 16 MHz

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- ESBMC
- Bound: 10 samples

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- Verification Failed

Failure due to a sum overflow (sum result = 2.0879 > 1).

Input sequence: {0.9995, -0.9995, 0.9995, 1, 1, 1, 0.9995, 0.9995, 0.9995, 0.9995, 1}

Redefine the implementation!

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Maintain the Representation

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- TDFII

Change the Realization Form
TDFII presents less sums and products

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Repeat the test

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- SUCCESS

The problem was solved

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- TDFII

- Verify limit cycle
- Verification time:3600
- MSP430 16-bit 16 MHz

- ESBMC
- Bound: 10 samples

But verifing limit cycles...

DSVerifier-Aided Verification Example

- $C(z) = \frac{0.2(z^2-2z+1)}{z^2-0.25}$

- $< 3,12 >$:3 bits for integer part and 12 bits for fractional part
- Dynamical Range: [-1,1]

- TDFII

- Verify limit cycle
- Verification time:3600
- MSP430 16-bit 16 MHz

- ESBMC
- Bound: 10 samples

- Verification Failed

Appears an oscillation: {-0.002, -0.002, -0.0015, -0.0015, -0.002, -0.002, -0.0015, -0.0015, -0.002, -0.002}.

Zero input sequence

Redefine the implementation!

DSVerifier-Aided Verification Example

- $C(z) = \frac{0.2(z^2-2z+1)}{z^2-0.25}$
- $< 3,4 >$:3 bits for integer part and 4 bits for fractional part
- Dynamical Range: [-1,1]
- TDFII
- Verify limit cycle
- Verification time:3600
- MSP430 16-bit 16 MHz
- ESBMC
- Bound: 10 samples

Verifying with a different representation...
There is a trade off: the oscillation is solved; however, there is an accurate loss

DSVerifier-Aided Verification Example

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- $< 3,4 >$:3 bits for integer part and 4 bits for fractional part
- Dynamical Range: [-1,1]
- TDFII
- Verify limit cycle
- Verification time:3600
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- ESBMC
- Bound: 10 samples
- SUCCESS

SUCCESS

DSVerifier Command-line Version

- The user provides the digital-system specification via an ANSI-C file
- Consider the following digital system: $H(z) = \frac{2.813z^2 - 0.0163z - 1.872}{z^2 + 1.068z + 0.1239}$

```
#include <dsverifier.h>

digital_system ds = {
  .b = {2.813, -0.0163, -1.872},
  .b_size = 3,
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→ Numerator Coefficients

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→ Number of Coefficients

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→ Denominator Coefficients

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implementation impl = {
   .int_bits = 4,
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```

- **Implementation aspects:**

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./dsverifier *<file>*
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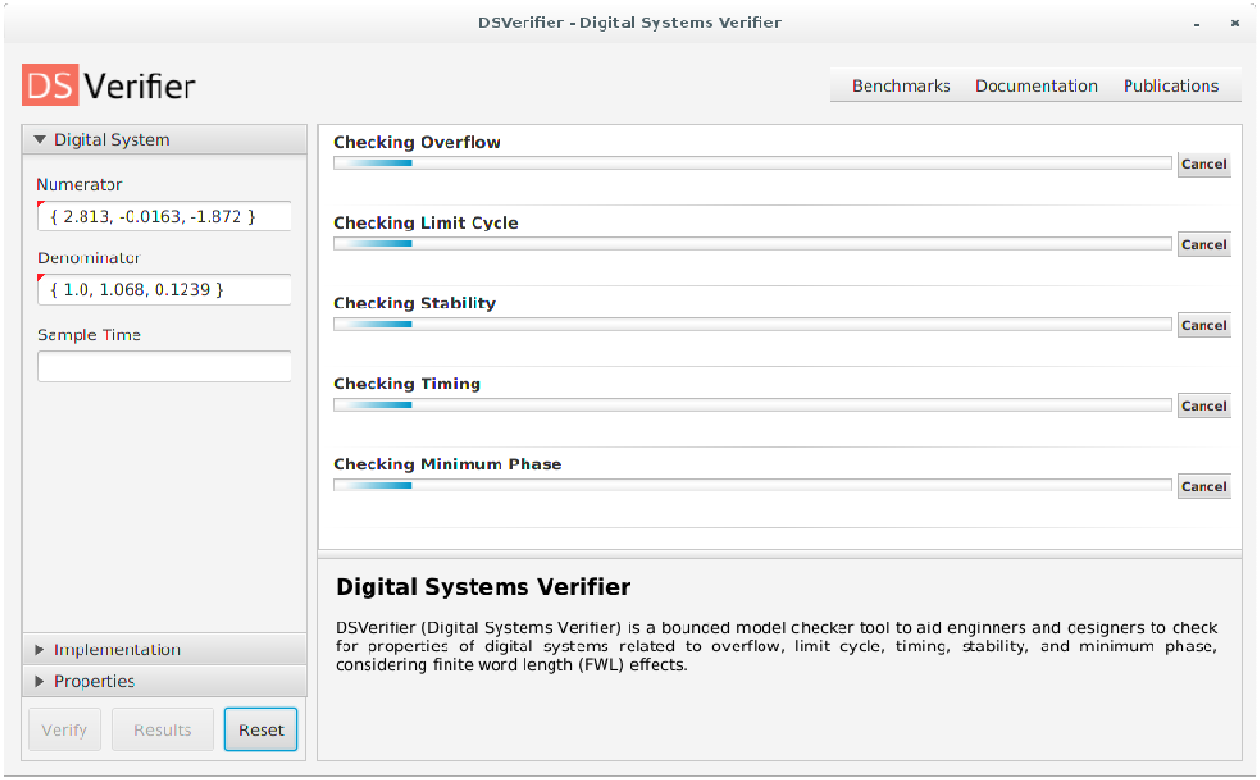
e.g., DFI, DFII

e.g., OVERFLOW

e.g., 10, 20, 30

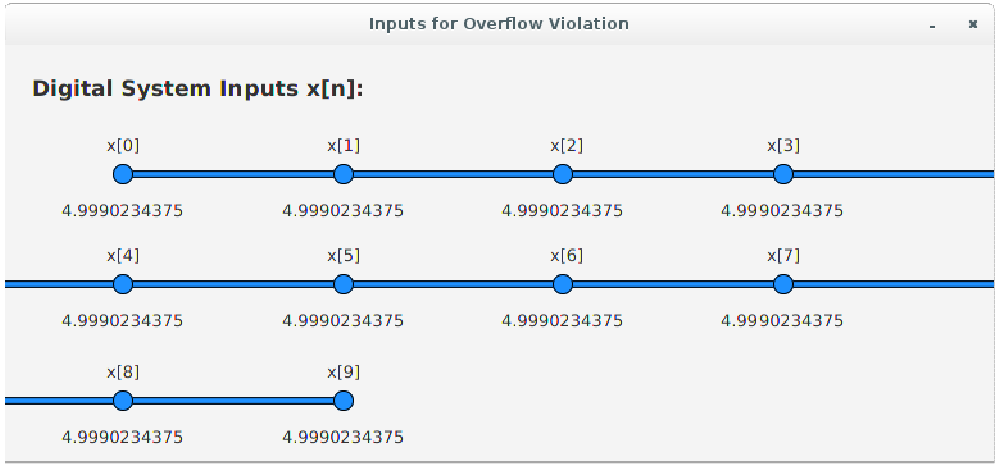
DSVerifier Usage (Graphical User Interface)

- The graphical user interface (GUI) improves usability and attracts more digital-system enginners
- Allows users to provide all required parameters for the verification
- Parallel execution of verification tasks, which is guided by properties



DSVerifier Usage (Graphical User Interface)

- Graphical verification results and counterexamples
- Access the documentation, benchmarks, and publications
- Developed using JavaFX
- Requires Java Runtime Environment Version 8.0 Update 40 (jre1.8.0 40)



Conclusions

- DSVerifier is able to verify digital systems and supports an extensive verification of different properties and realization forms
- DSVerifier can be regarded as an automated and reliable tool if compared to traditional simulation tools
  - An enginner can verify during design phase, if the digital-system presents the expected behavior

Future Work

- Support for closed-loop system verification, more system-level properties, realizations, hardware platforms, and BMC tools
- Source code, benchmarks, experimental results, and publications are available at **http://www.dsverifier.org**

Demonstration