





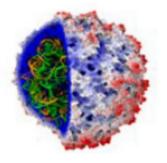
31st ACM/SIGAPP Symposium on Applied Computing

SMT-Based Context-Bounded Model Checking for CUDA Programs

Phillipe Pereira, Higo Albuquerque, Hendrio Marques, Isabela Silva, Vanessa Santos, Celso Barbosa, Ricardo Ferreira, and **Lucas Cordeiro**



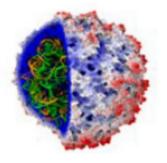






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 - > specially those that require high computational power



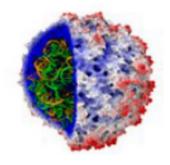


Developed by NVIDIA to configure GPUs TVIDIA.



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- Currently used in:
 - **>** biomedicine
 - > air traffic control
 - > weather simulation



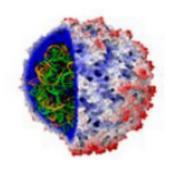


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- initially used in graphical processing in games applications
 - > specially those that require high computational power
- Currently used in:
 - ➤ biomedicine
 - > air traffic control
 - > weather simulation
- We need to ensure code correctness in safety-critical GPU applications





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Array out-of-bounds due to incorrect access in unallocated memory region



```
int a[2];
...
kernel(int *a){
    if(a[1]==1)
        a[threadIdx.x+2] = threadIdx.x;
    else
        a[threadIdx.x] = threadIdx.x;
}
```

Exploit SMT-based context-BMC to verify CUDA-based programs

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- Develop an operational model for the CUDA platform (named COM)
 - Integrate COM into the Efficient SMT-Based Context-Bounded Model Checker (ESBMC) (TSE'12)
- Apply context-bounded model checking based on the Satisfiability Modulo Theories (SMT)
 - Monotonic Partial Order Reduction (MPOR) (CAV'09)

Exploit SMT-based context-BMC to verify CUDA-based programs

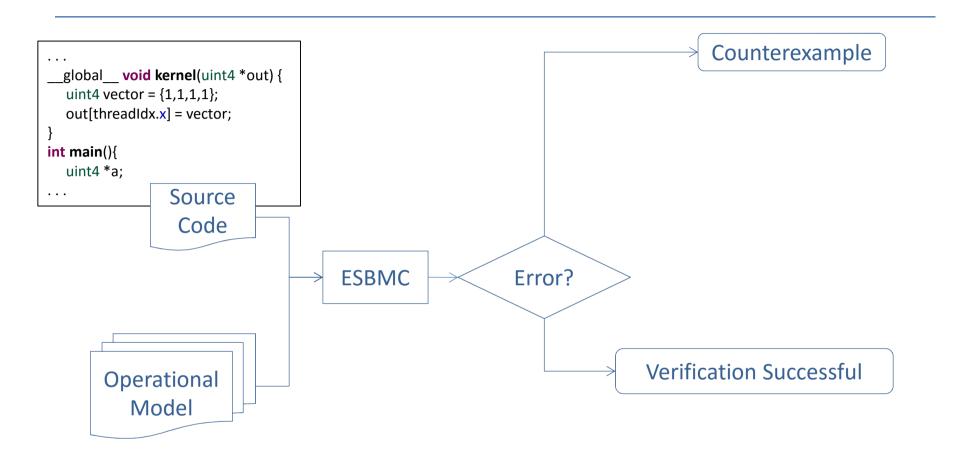
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 - Monotonic Partial Order Reduction (MPOR) (CAV'09)
- Compare ESBMC-GPU experimental results with other state-of-art software verifiers for CUDA

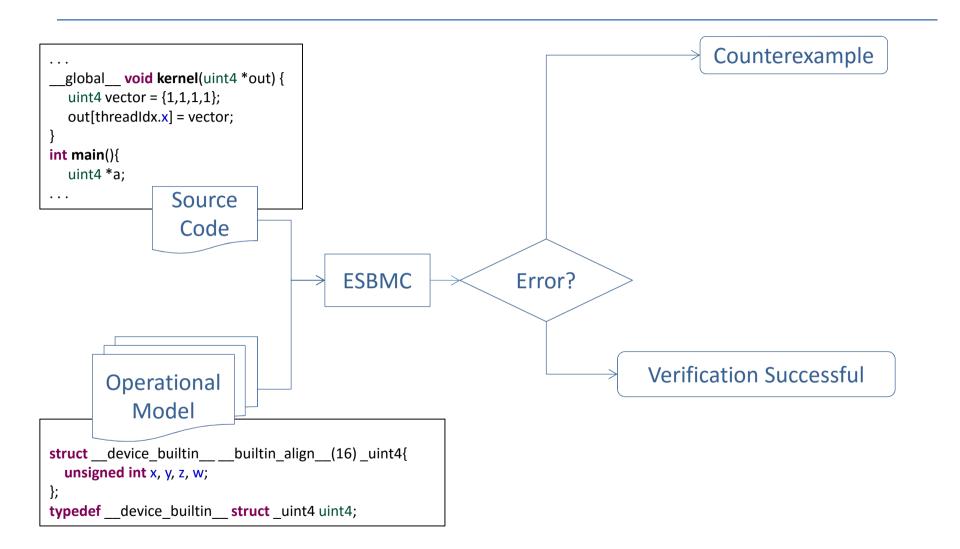
- COM aims to
 - Abstractly represent the associated CUDA libraries
 - > checks **pre-** and **post-conditions**
 - > simulates **behavior**
 - Reduce verification effort
 - by only checking relevant behavior

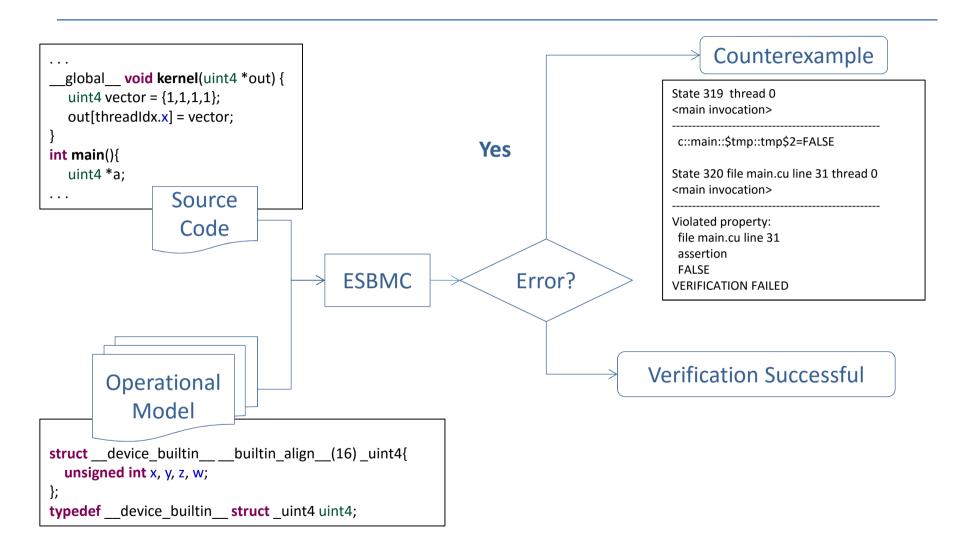
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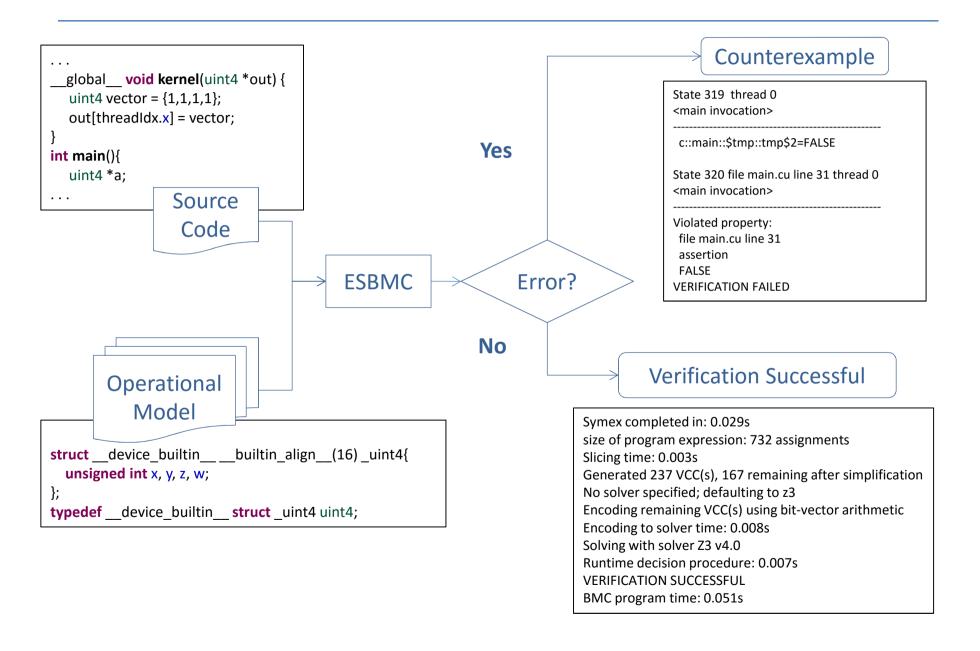
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 - ➤ ESBMC++ (ECBS'13) and ESBMCQtOM (SPIN'16)
- CUDA is a proprietary platform
 - CUDA Programming Guide and IDE Nsight









```
#include <cuda.h>
#include <stdio.h>
#define N 2
  _global___ void definitions(int* A){
        atomicAdd(A,10);
int main (){
        int a = 5;
        int *dev_a;
        cudaMalloc ((void**) &dev_a, sizeof(int));
        cudaMemcpy(dev_a, &a,
sizeof(int),cudaMemcpyHostToDevice);
        ESBMC_verify_kernel(definitions,1,N,dev_a);
        cudaMemcpy(&a,dev_a,sizeof(int),cudaMemcpyD
eviceToHost):
        assert(a==25);
        cudaFree(dev_a);
        return 0;
```

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        cudaFree(dev_a);
        return 0;
```

```
# cudaMalloc
cudaError_t cudaMalloc(void ** devPtr, size_t size) {
       cudaError_t tmp;
          ESBMC_assert(size > 0, "Size to be allocated must be greater than zero");
        *devPtr = malloc(size);
        if (*devPtr == NULL) {
                 tmp = CUDA ERROR OUT OF MEMORY;
                 exit(1);
         } else {
                 tmp = CUDA SUCCESS:
          _ESBMC_assert(tmp == CUDA_SUCCESS, "Memory was not allocated");
        lastError = tmp;
        return lastError;
```

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```

simulate behavior

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```

- Verification model adopts the CPU parallel processing
 - Using the Pthread/POSIX library

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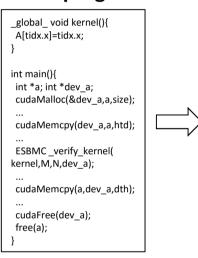
CUDA program

```
_global_void kernel(){
    A[tidx.x]=tidx.x;
}

int main(){
    int *a; int *dev_a;
    cudaMalloc(&dev_a,a,size);
    ...
    cudaMemcpy(dev_a,a,htd);
    ...
    ESBMC_verify_kernel(
    kernel,M,N,dev_a);
    ...
    cudaMemcpy(a,dev_a,dth);
    ...
    cudaFree(dev_a);
    free(a);
}
```

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CUDA program



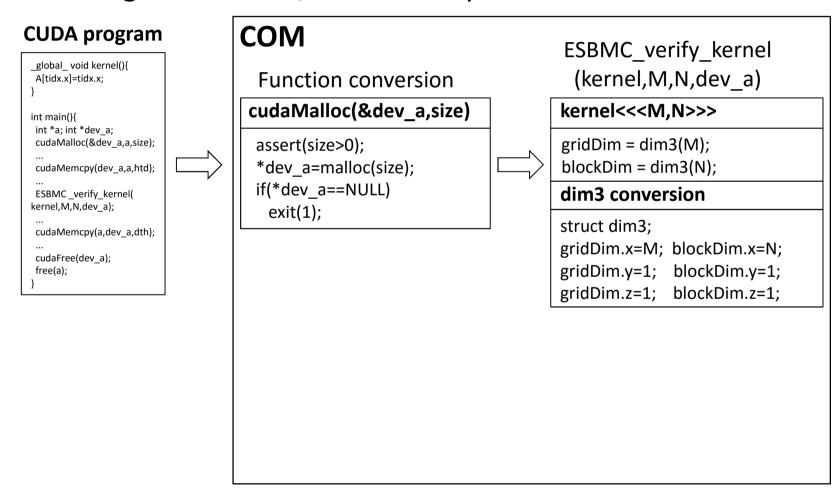
COM

Function conversion

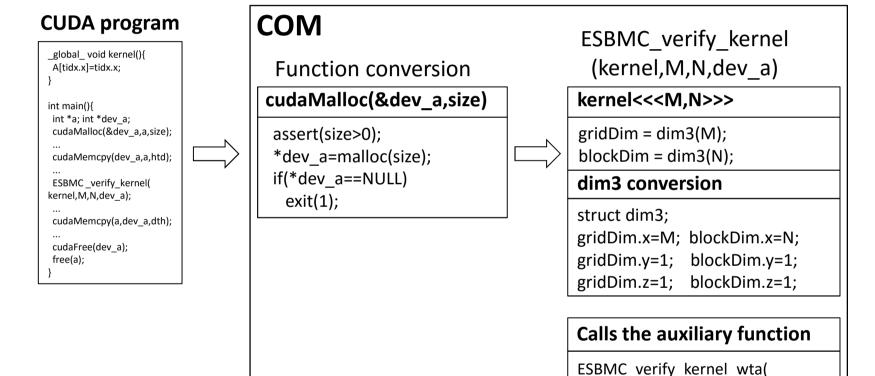
```
cudaMalloc(&dev_a,size)
```

```
assert(size>0);
*dev_a=malloc(size);
if(*dev_a==NULL)
  exit(1);
```

- Verification model adopts the CPU parallel processing
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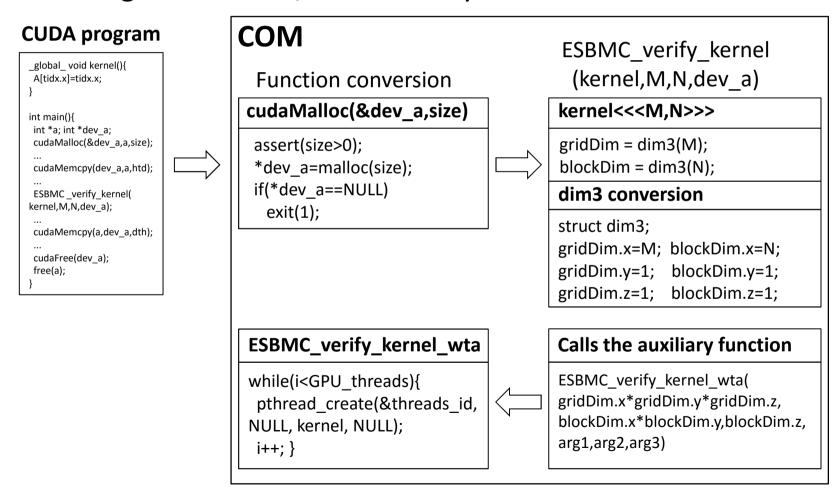
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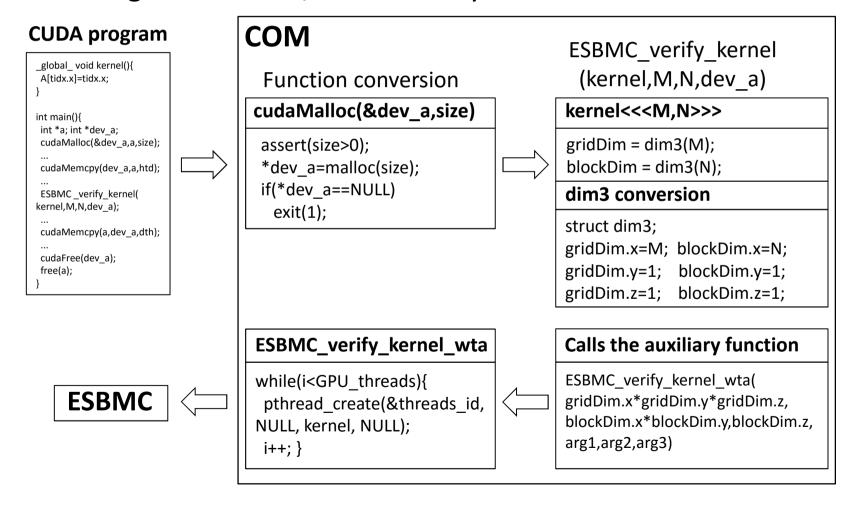
gridDim.x*gridDim.y*gridDim.z, blockDim.x*blockDim.y,blockDim.z,

arg1, arg2, arg3)

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Monotonic Partial Order Reduction (MPOR)

- MPOR classifies thread transitions in a multithreaded program
 - Each transition may be dependent or independent
 Identify interleaving pairs which result in the same state

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- MPOR classifies thread transitions in a multithreaded program
 - Each transition may be dependent or independent
 Identify interleaving pairs which result in the same state
- First application of the technique to verify CUDAbased programs
 - Reduction in time and verification effort
 - Elimination of threads interleavings that access different array positions

MPOR Applied to CUDA-based Programs

- MPOR algorithm in the ESBMC-GPU
- **1. function** MPOR (v, π)
- 2. Check whether s_i exists in π ; otherwise, go to step 4
- 3. Check whether A_i produces a new state in π ; otherwise, go to step 5
- 4. Analyze whether $\gamma(s_{i-1}, s_i)$ is independent on π ; otherwise, go to step 6
- 5. Return "independent" on π and terminates
- 6. Return "dependent" on π and terminates
- 7. end function

MPOR algorithm in the ESBMC-GPU

- 1. function MPOR (v, π) $\pi = \{v_0,...,v_k\}$
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 $\mathbf{v} = (A_i, C_i, s_i)$ A_i : active thread C_i : context switch S_i : current state

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7. end function

```
kernel1(int *a){
a[threadIdx.x] = threadIdx.x;
v_0: t_0, 0, a[0] = 0, a[1] = 0
```

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kernel1(int *a){
a[threadIdx.x] = threadIdx.x;
v_0: t_0, 0, a[0] = 0, a[1] = 0
v_1: t_1, 1, a[0] = 0, a[1] = 0
```

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```
kernel1(int *a){
    a[threadIdx.x] = threadIdx.x;
}

threadIdx.x=0

v_0: t_0, 0, a[0] = 0, a[1] = 0

v_1: t_1, 1, a[0] = 0, a[1] = 0

threadIdx.x=1

v_2: t_2, 2, a[0] = 0, a[1] = 1
```

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kernel1(int *a){
    a[threadIdx.x] = threadIdx.x;}

t_1 \rightarrow t_2
s_2: a[0] = 0
    a[1] = 1

v_0: t_0, 0, a[0] = 0, a[1] = 0

v_1: t_1, t_2
v_3: t_1, t_2
v_3: t_4: t_2
v_3: t_4: t_2: t_4: t_
```

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kernel1(int *a){
    a[threadIdx.x] = threadIdx.x;}

Dependent
    t_1 \rightarrow t_2
    s_2: a[0] = 0
    a[1] = 1

where all dx.x = 0

v_0: t_0, 0, a[0] = 0, a[1] = 0

threadIdx.x = 0

v_1: t_1, t_1, t_2[0] = 0, t_2[1] = 0

threadIdx.x = 1

v_2: t_2, t_2, t_2, t_3[1] = 1
```

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kernel1(int *a){
    a[threadIdx.x] = threadIdx.x;
}

Dependent
t_1 \rightarrow t_2
s_2: a[0] = 0
a[1] = 1

threadIdx.x=1
v_0: t_0, 0, a[0] = 0, a[1] = 0
v_0: t_0, v_0: v_0:
```

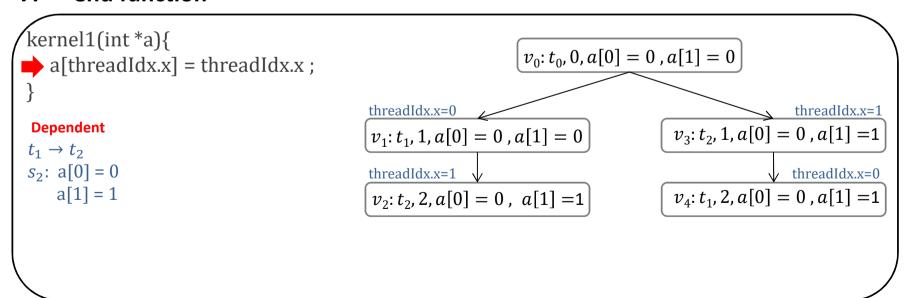
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```
kernel1(int *a){
                                                                     v_0: t_0, 0, a[0] = 0 , a[1] = 0
   a[threadIdx.x] = threadIdx.x;
                                               threadIdx.x=0
                                                                                                           threadIdx.x=1
Dependent
                                                                                          v_3: t_2, 1, a[0] = 0, a[1] = 1
                                                v_1: t_1, 1, a[0] = 0, a[1] = 0
         t_2 \rightarrow t_1
t_1 \rightarrow t_2
s_2: a[0] = 0 s_2: a[0] = 0
                                               threadIdx.x=1
                                                                                                          threadIdx.x=0
    a[1] = 1
                     a[1] = 1
                                                                                          v_4: t_1, 2, a[0] = 0, a[1] = 1
                                                v_2: t_2, 2, a[0] = 0, a[1] = 1
```

 $\mathbf{v} = (A_i, C_i, s_i)$

A_i: active threadC_i: context switch

s_i: current state

MPOR algorithm in the ESBMC-GPU

- 1. function MPOR (v, π) $\pi = \{v_0,...,v_k\}$
- 2. Check whether s_i exists in π ; otherwise, go to step 4
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```
kernel1(int *a){
                                                                     v_0: t_0, 0, a[0] = 0 , a[1] = 0
   a[threadIdx.x] = threadIdx.x;
                                               threadIdx.x=0
                                                                                                           threadIdx.x=1
Dependent
                                                                                          v_3: t_2, 1, a[0] = 0, a[1] = 1
                                                v_1: t_1, 1, a[0] = 0, a[1] = 0
t_1 \rightarrow t_2
         t_2 \rightarrow t_1
s_2: a[0] = 0 s_2: a[0] = 0
                                               threadIdx.x=1
                                                                                                          threadIdx.x=0
   a[1] = 1
                     a[1] = 1
                                                                                          v_4: t_1, 2, a[0] = 0, a[1] = 1
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```

 $\mathbf{v} = (A_i, C_i, s_i)$

 A_i : active thread

s_i: current state

 C_i : context switch

MPOR algorithm in the ESBMC-GPU

- 1. function MPOR (v, π) $\pi = \{v_0, ..., v_k\}$
- 2. Check whether s_i exists in π ; otherwise, go to step 4
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```
kernel1(int *a){
                                                                   v_0: t_0, 0, a[0] = 0 , a[1] = 0
   a[threadIdx.x] = threadIdx.x;
                                              threadIdx.x=0
Dependent
                                                                                         v_3: t_2, 1, a[0] = 0, a[1] = 1
                                               v_1: t_1, 1, a[0] = 0, a[1] = 0
         t_2 \rightarrow t_1
t_1 \rightarrow t_2
s_2: a[0] = 0 s_2: a[0] = 0
                                              threadIdx.x=1
                                                                                       v_4: t_1, 2, a[0] = 0, a[1] = 1
   a[1] = 1
                     a[1] = 1
                                               v_2: t_2, 2, a[0] = 0, a[1] = 1
                                                     t_1 \rightarrow t_2 or t_2 \rightarrow t_1 result in the same state,
                                                     this is an independent transition
```

MPOR algorithm in the ESBMC-GPU

- 1. function MPOR (v, π) $\pi = \{v_0, ..., v_k\}$
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7. end function

```
kernel (int *a)  if(a[1]==1)   a[threadIdx.x+2] = threadIdx.x;  else  a[threadIdx.x] = threadIdx.x;
```

 $\mathbf{v} = (A_i, C_i, s_i)$ A_i : active thread C_i : context switch S_i : current state

MPOR algorithm in the ESBMC-GPU

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7. end function

```
kernel (int *a)

if(a[1]==1)

a[threadIdx.x+2] = threadIdx.x;

else

a[threadIdx.x] = threadIdx.x;
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- 4. Analyze whether $\gamma(s_{i-1}, s_i)$ is independent on π ; otherwise, go to step 6
- 5. Return "independent" on π and terminates
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```
kernel (int *a)
if(a[1]==1)
a[threadIdx.x+2] = threadIdx.x ;
else
a[threadIdx.x] = threadIdx.x;
v_0: t_0, 0, a[0] = 0, a[1] = 0
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```
kernel (int *a)  if(a[1] == 1) \\ a[threadIdx.x + 2] = threadIdx.x; \\ else \\ a[threadIdx.x] = threadIdx.x; \\ \frac{threadIdx.x = 0}{v_1: t_1, 1, a[0] = 0, a[1] = 0} \\ \frac{threadIdx.x = 0}{v_1: t_1, 1, a[0] = 0, a[1] = 0} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[1] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[0] = 1} \\ \frac{threadIdx.x = 1}{v_2: t_2, 2, a[0] = 0, a[0]
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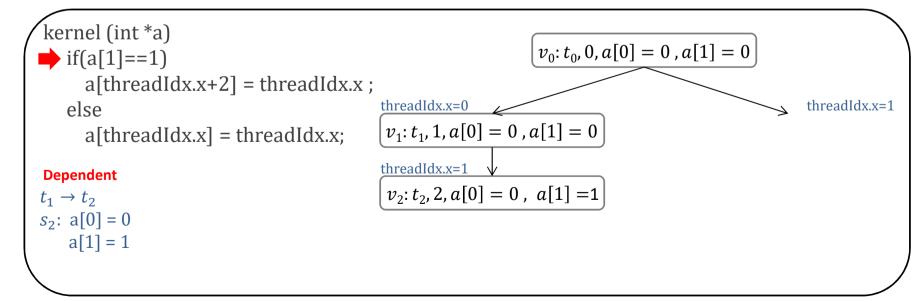
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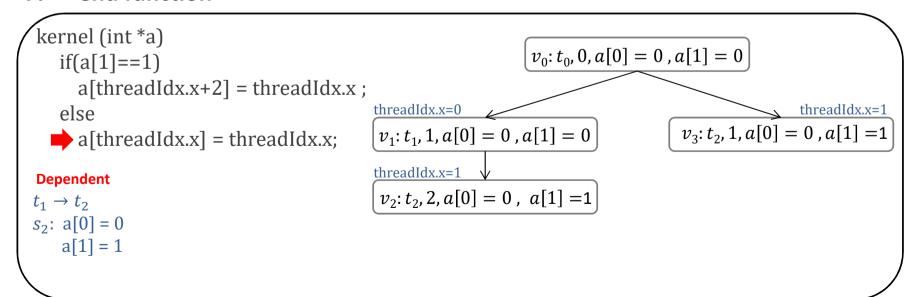
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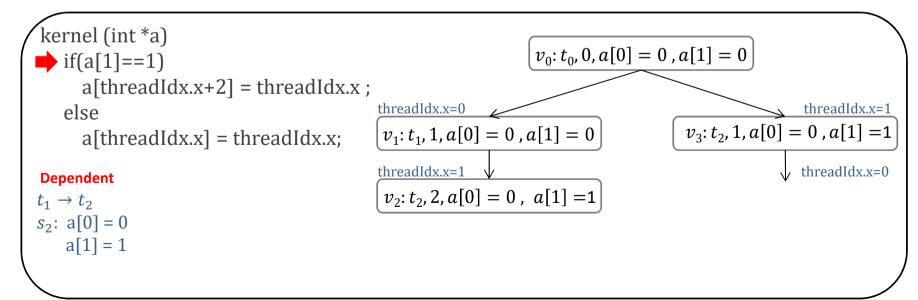
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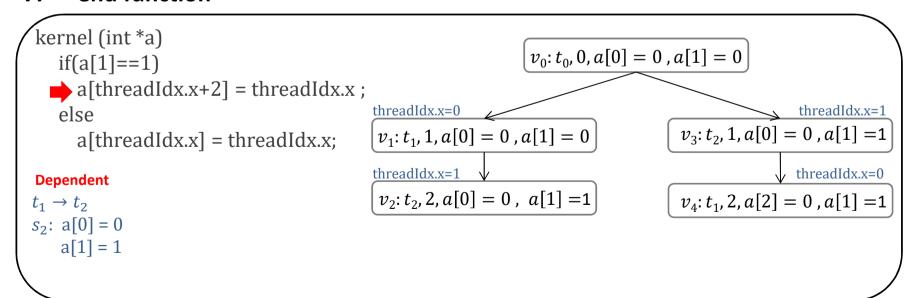
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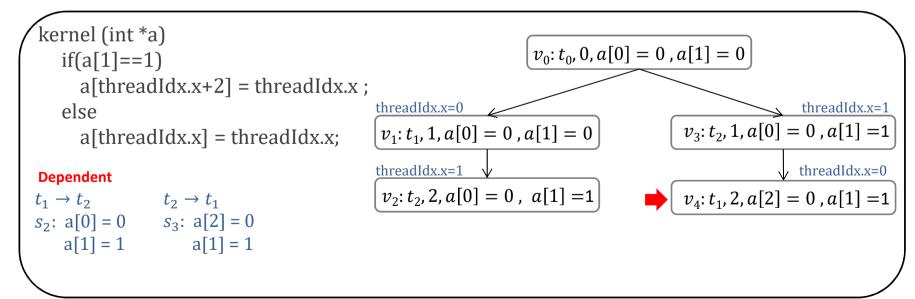
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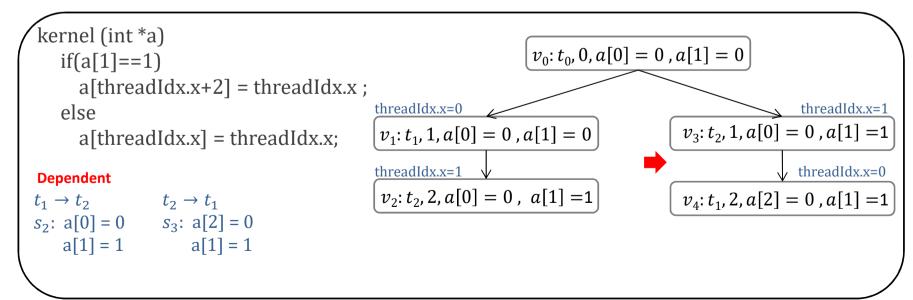
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```
kernel (int *a)
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   if(a[1]==1)
      a[threadIdx.x+2] = threadIdx.x;
                                              threadIdx.x=0
                                                                                                         threadIdx.x=1
   else
                                                                                        v_3: t_2, 1, a[0] = 0, a[1] = 1
                                               v_1: t_1, 1, a[0] = 0, a[1] = 0
      a[threadIdx.x] = threadIdx.x;
                                               threadIdx.x=1
                                                                                                      threadIdx.x=0
Dependent
                                               v_2: t_2, 2, a[0] = 0, a[1] = 1
                                                                                        v_4: t_1, 2, a[2] = 0, a[1] = 1
t_1 \rightarrow t_2 t_2 \rightarrow t_1
s_2: a[0] = 0 s_3: a[2] = 0
                                                     t_1 \rightarrow t_2 computes a different state of t_2 \rightarrow t_1,
   a[1] = 1
                     a[1] = 1
                                                     resulting in dependent transitions
```

Two-threads Analysis

Reduction for two-threads during the program verification

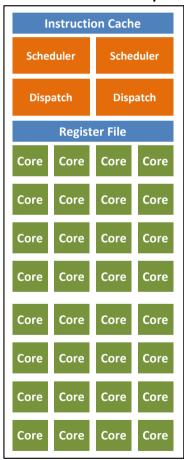
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 - If an error is found between 2 threads in a block, it will also be found for more threads
 - This proposition holds due to the GPU architecture

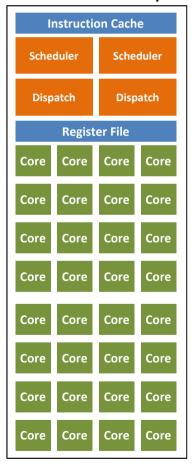
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 - This technique is also used by other GPU kernel verification tools (e.g., GPUVerify and PUG)

Fermi - Stream Multiprocessor

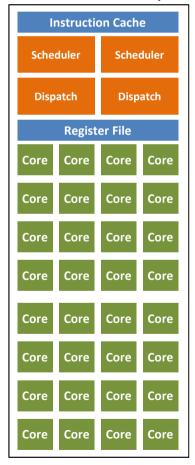


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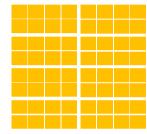


Warp (32 threads)

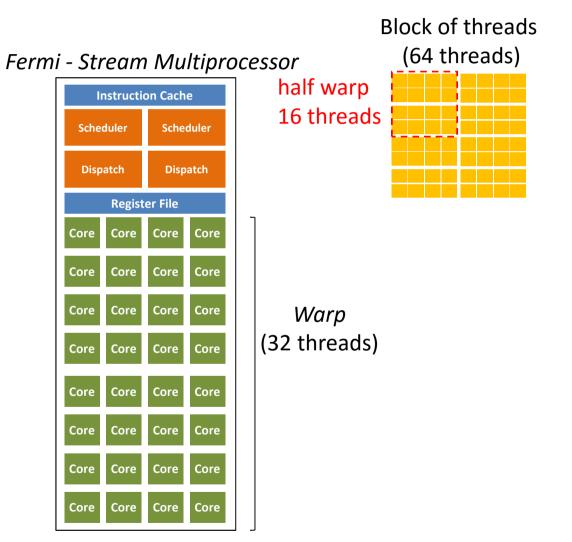
Fermi - Stream Multiprocessor



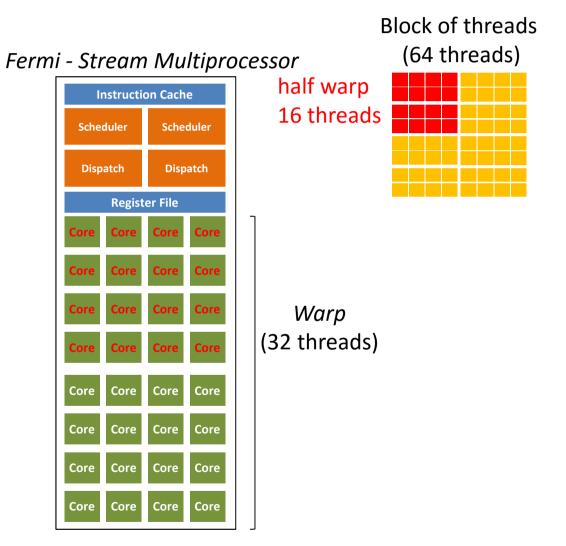
Block of threads (64 threads)

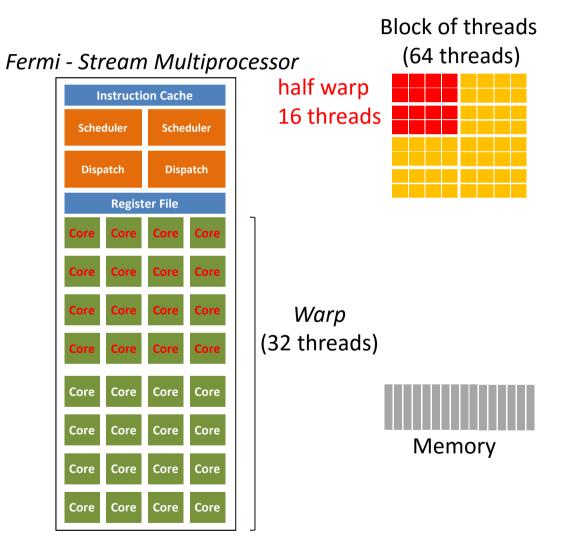


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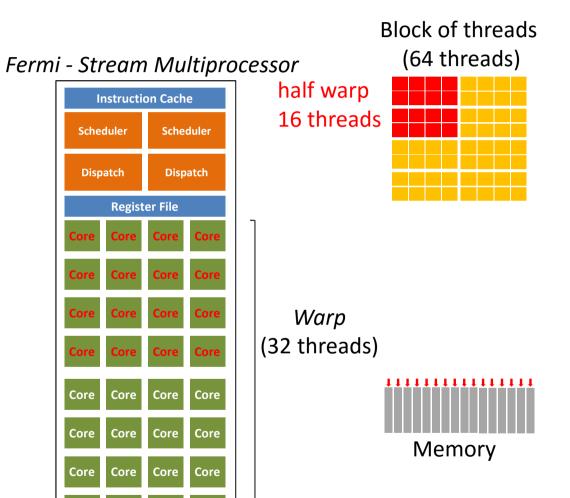


One thread group is processed by a half warp in the SM





Two-threads Analysis in Fermi



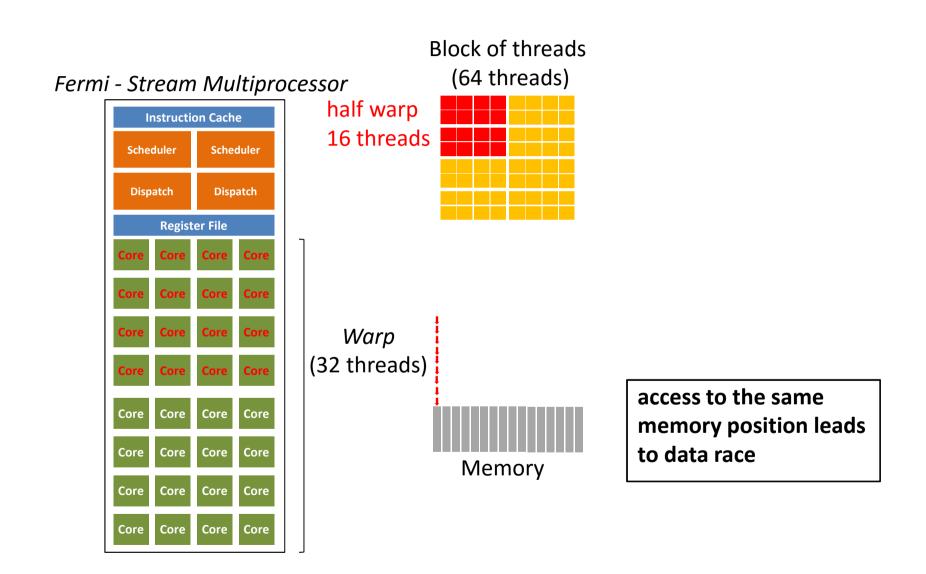
Core

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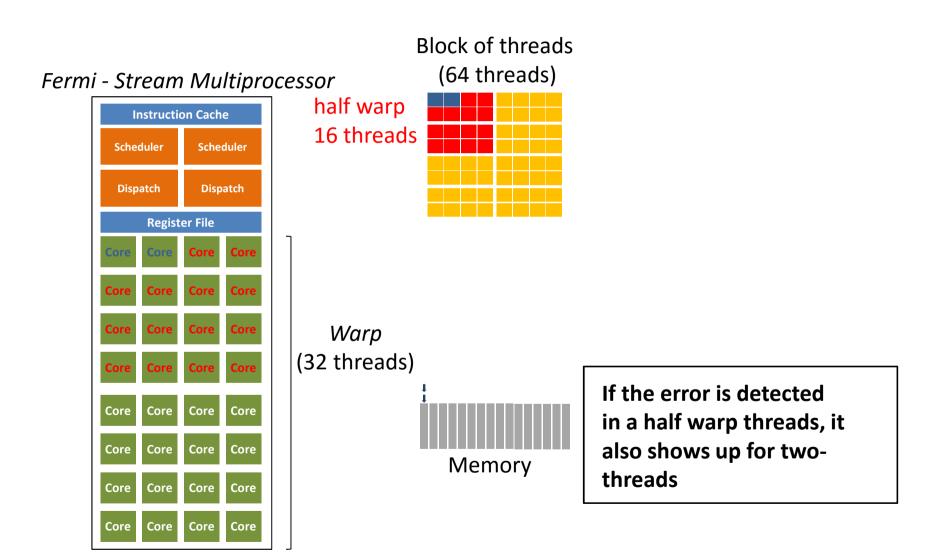
Core

there is no data race to access different memory positions

Two-threads Analysis in Fermi



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- Standard PC desktop, time-out 900 seconds

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 - CUDA intrinsic variables (e.g., uint4)

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 - supports MPI, POSIX, OpenMP, CUDA, and C11

- GPUVerify checks data race and barrier divergence
 - There is no support for the main function
- PUG checks data races, barrier synchronization, and conflicts with shared memory
- GKLEE is based on concrete and symbolic execution
 - Supports the verification of barriers synchronization and race condition
- **CIVL** is a framework for static analysis and concurrent program verification
 - supports MPI, POSIX, OpenMP, CUDA, and C11
 - symbolic execution, POR, and GPU threads with Pthread

Result\Tool	ESBMC- GPU	GKLEE	GPUVERIFY	PUG	CIVL
True Correct	60	53	58	39	23
False Correct	67	56	30	15	24
True Incorrect	1	14	9	7	0
False Incorrect	3	7	8	11	3
Not supported	23	24	49	82	104
Time(s)	811	128	147	12	158

Result\Tool	ESBMC- GPU	GKLE	E	GPUVERIFY	PUG	CIVL
True Correct	60	53		58	39	23
Total number of I which the progra				30	15	24
contain errors	-	±-7		9	7	0
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True Correct	60	53		58	39	23
False Correct	67	56		30	15	24
Total number of which the error i				9	7	0
was found and a was reported	n error pa	th		8	11	3
Not supported	23	23 24		49	82	104
Time(s)	811	128		147	12	158

Result\Tool	ESBMC- GPU	GKLEE	GPUVERIFY	PUG	CIVL
True Correct	60	53	58	39	23
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False Incorrect	pointer, a assertion	nd user-s	11	3	
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True Correct	60		53	58	39	23
in which an error	nber of benchmarks an error is reported gram that fulfills the tion		56	30	15	24
for a program that specification			14	9	7	0
False Incorrect	3		7	8	11	3
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 Proposed a software verifier, which is able to check CUDA-based programs

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- Future work
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 - Techniques to reduce interleavings (lazy sequentialization)