# Verifying Digital Systems with MATLAB (Tool Demo)

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"...guaranteeing the correctness of cyber-physical systems (CPS) remains an a stounding challenge"

Xi Zheng *et al.,* 2014.

*"Simulation alone is not sufficient to support verification and validation of CPS."* 



# Step A

DSVerifier builds an ANSI-C code representation of the digital system based on the specification.

Step B

DSVerifier formulates a FWL model based on fixedpoint arithmetic:

$$\mathsf{FWL} [\bullet] : \mathfrak{R} \longrightarrow \mathsf{Q}[\mathfrak{R}]$$

# Step C

### **DSVerifier checks a property** $\Phi$ **up to a bound** *k*:

| Φ                  | Bits < I, F >   | Result   |
|--------------------|-----------------|----------|
| Quantization error | 32-bits <15,16> | >1%      |
|                    | 16-bits <7,8>   | >1%      |
|                    | 8-bits <3,4>    | <1%      |
| Stability          | 8-bits <3,4>    | Unstable |

# Approach and Uniqueness

### **Bounded model checking**

Translate the model into a VC  $\psi$  such that:

 $\psi$  is satisfiable iff  $\varphi$  has counterexample of max. depth k



# DSVerifier Toolbox

#### 🔵 🔲 DSVerifier App

| riansier Function  | Ciosed-Loop             | State-Space |  |  |
|--|-------------------------|-------------|--|--|
| Closed-Loop Representation   |                         |             | Implementation   |  |
| Plant  |                         |             | Integer Bits 12  Fractional Bits 3   |  |
| Numerator [1 -1 -2]  |                         |             |  |  |
| Denominator [11  | Denominator [1 1 0.576] |             | max range 1 — min range -1 —   |  |
| Controller   |                         |             | Delta  |  |
| Numerator [1 0.576 0.927]  |                         |             | Timeout 3600   |  |
| Denominator [1-4.867 0.736]<br>Sample Time 0.02<br>Configurations<br>BMC ESBMC<br>Solver Boolector<br>Overflow Mode Wrap-Around<br>Rounding Mode Round |                         |             | Realization Form DFII  |  |
|  |                         |             | K bound  |  |
|  |                         | )           | 0 10 20 30 40 50 60 70 80 90 100<br>Properties                                   |  |
|  |                         | )<br>)<br>) | <ul> <li>Stability</li> <li>✓ Limit Cycle</li> <li>Quantization Error</li> </ul> |  |
| Error Mode   | Absolute 🔻              | •)          | Reset Verify   |  |

# **Contributions**

**i.** support for transfer-function and state-space representations in open- and closed-loop form;

# Step 2

## Numerical representation < *I* , *F* >:

- *I* is the integer part and
- **F** is the fractional part

## Step 3

### **Setup verification:**

- choose a property Φ;
- a maximum
   verification time;
- a bound k;
- a BMC tool.

implementation <3,4>
states = 3;
inputs = 1;
outputs = 1;
A = [...]
B = [...]
C = [...]
D = [...]

stability;

**Properties:** 

- quantization error;
- controllability;
- observability;

**ii.** verify different numerical representations and realization forms of digital systems;

**iii.** provide a MATLAB toolbox to check specific properties of digital systems while taking into account FWL;

### As future work:

- verify uncertainties in digital systems represented by state-space;
- integrate counterexample reproducibility for digital systems



For further information, publications, and downloads, see: http://www.dsverifier.org/