

SMT-based Bounded Model Checking for Multi-threaded Software in Embedded Systems

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Embedded systems are ubiquitous School of Electronics and Computer Science but their verification becomes more difficult.

- functionality demanded increased significantly
 - peer reviewing and testing
- multi-core processors with scalable shared memory
 - but most verification tools focus on message passing

Scalability and Precision South Sout

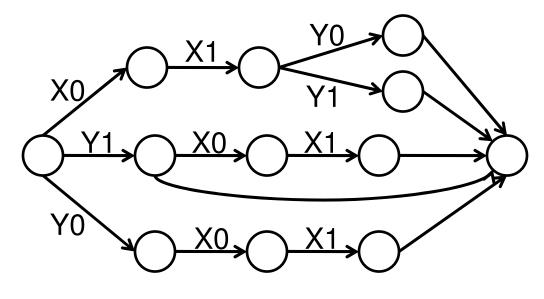


- state space explosion problem
 - exploit proof of unsatisfiability
 - integrate POR with symbolic algorithms
 - \rightarrow visible instruction and read-write analysis
- precision of arithmetic and bit-level operations
 - use decision procedures of QF formulae with a more accurate model of the ANSI-C semantics (SMT)
 → combine different background theories and solvers

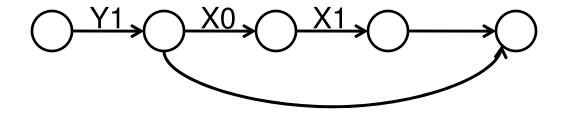
Can an algorithmic method reason accurately about multi-threaded software in embedded systems by controlling the verification complexity?

SMT-based Verification of Multi-threaded Software

Lazy exploration of interleavings



↓ After reduction

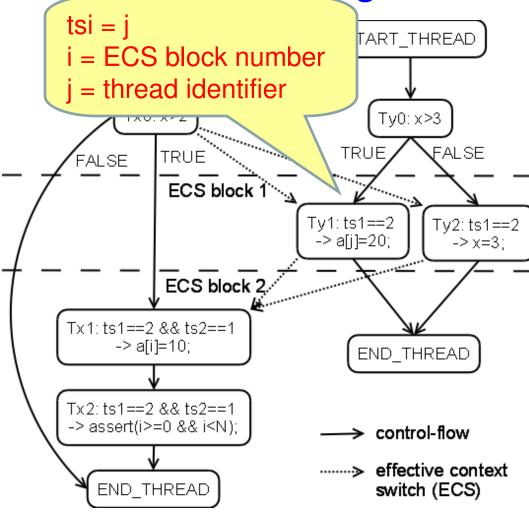




#define N 10 int a [N], i, j =1, x=2; void *Tx(void *arg) { if (x>2) { a[i] = *((int *)arg); //X0 assert(i>=0 && i<N); //X1 } void *Ty(void *arg) { if (x>3) a[j]=*((int *)arg); //Y0 else x=3; //Y1 } int main(void) { int arg1=10, arg2=20; i=nondet_uint(); //create Tx with arg1 //create Ty with arg2 }

SMT-based Verification of Multi-threaded Software

Scheduling Recording





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UNIVERSITY OF SMT-based Verification Southampton School of Electronics and Computer Science of Multi-threaded Software #define N 10 **Under-approximation & Widening** int a [N], i, j =1, x=2; void *Tx(void *arg) { if (x>2) { START THREAD START THREAD ((int *)arg); //X0 ly = (ts1 == 2)>=0 && i<N); //X1 Ix = (ts1 == 2) && (ts2 == 1)ly -> x=3 Ty0: x>3 |x -> a[i] = 10FALSE $Ix \rightarrow assert(i \ge 0 \&\& i < N)$ void *Ty(void *arg) { if (x>3) Ty1: ts1==2 Ty2: ts1==2 a[j]=*((int *)arg); -> a[i]=20: //Y0 ->x=3: else ECS block 2. //Y1 x=3; Tx1: ts1==2 && ts2==1 -> a[i]=10; END THREAD int main(void) { int arg1=10, arg2=20; Tx2: ts1==2 && ts2==1 i=nondet_uint(); -> assert(i>=0 && i<N); control-flow //create Tx with arg1 //create Ty with arg2 ······ ⇒ effective context END_THREAD switch (ECS)

Experimental Evaluation



- described and evaluated SMT-based BMC in large embedded software
 - SMT-based BMC is more efficient than SAT-based BMC (but not uniformly)
 - introduced continuous verification for large systems
- evaluated the UW, schedule recording, and lazy approaches
 - add concurrency constraints lazily
 → extremely fast for satisfiable instances
 - memory overhead and slowdowns to extract the unsatisfiable cores

Results



- built and evaluated first SMT-based BMC for ANSI-C
- UW, lazy and schedule recording algorithms
- introduced continuous verification approach
- users.ecs.soton.ac.uk/lcc08r/esbmc/

Future Work

- partial order reduction (static and dynamic)
- data races detection (compatibility with compiler)
- Craig interpolation to generate threads scheduling